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Investigation of Breakdown Location in GaAs MESFETs by Two-Dimensional Simulation and Emission Microscopy

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Breakdown in a WSi self-aligned-gate GaAs MESFET has been simulated by self-consistent two-dimensional numerical calculations. The location of breakdown in the device has been found to have a specific gate-bias dependence: For open channel bias condition impact ionisation is initiated at the n^+ to channel implant interface, under pinch-off condition however at the gate contact edges. These results have been experimentally verified by the light emission characteristics of the FET which were measured by high-resolution emission microscopy.

1. INTRODUCTION

In GaAs power FETs the optimum tradeoff between high drain current and high breakdown voltage is essential in achieving high output power. This is especially critical for high frequency applications for which device dimensions have to be shrinked. Hence many attempts have been made to attain a better understanding of the physics governing the breakdown mechanisms[1,2].

Impact ionisation is generally assumed to be the cause of breakdown in MESFETs. In this study we use the two-dimensional device simulator MINIMOS to identify the regions where impact ionization occurs in real self-aligned FETs. The validity of the simulated results have been investigated experimentally by high resolution emission spectroscopy.

2. BREAKDOWN SIMULATION

MINIMOS is amongst the few MESFET simulation programs which are capable of treating the generation of carriers in a fully self-consistent manner[2]. Furthermore, the fundamental semiconductor equations for both carrier types are solved. This means that the breakdown behaviour can be calculated much more accurately than in the majority of contemporary numerical models which have to resort to treating the breakdown phenomena as a one-dimensional, one-carrier problem.

The generation rate G of electron-hole pairs due to the mechanism of impact ionisation is modelled as:

$$G = \alpha_n \cdot |J_n|/q + \alpha_p \cdot |J_p|/q \qquad (1)$$

J_n, J_p are the electron and hole current densities respectively. α_n, α_p are the ionisation rates of the mobile charge carriers. These rates are strongly dependent upon the magnitude of the electric field acting in the direction of the current vector[2,3] and upon the values chosen for the ionisation coefficients[4]; in this study values from Sze and Gibbons[5] were used. Surface states and their influence on electric field distribution was modelled as outlined previously[6].

3. DEVICE STRUCTURE

The structure of the device which was studied is shown in Fig. 1.

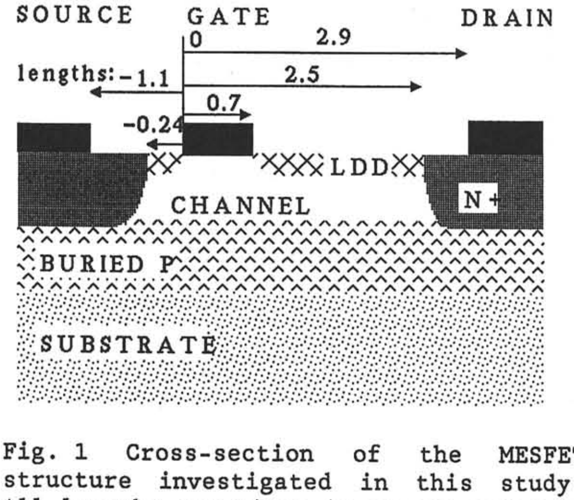


Fig. 1 Cross-section of the MESFET structure investigated in this study. All lengths are given in µm and refer to the length scale in Figs. 2 and 3.

This has been fabricated with a WSi self-aligned process[9] using an asymmetrical n^+ contact-implant as indicated in fig. 1. Previous work[2] has been extended to include all implants used in the FET processing (buried p, LDD and contact implants).

4. SIMULATION RESULTS

Simulations have revealed that the location of high carrier generation from impact ionisation varies with the gate bias conditions (Figs. 2 and 3). For V_{gs} = 0 V the peak of the generation rate appears at the interface of channel and n^+ implants in the region between drain and gate contacts (Fig. 2).

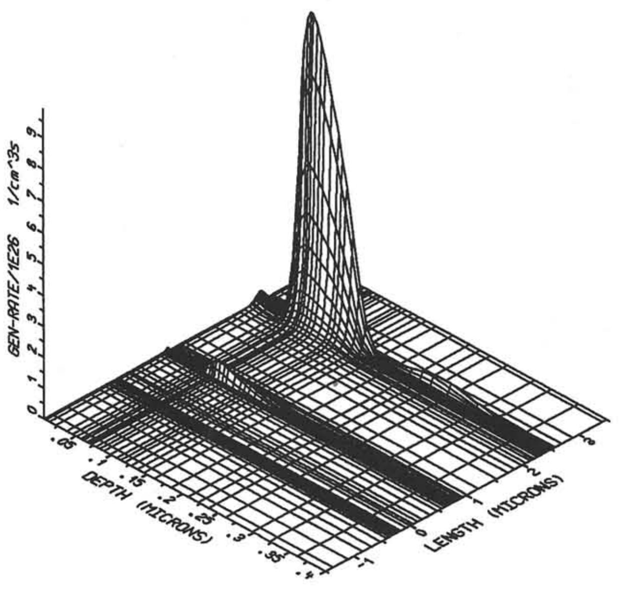


Fig. 2 Avalanche generation rate for Vgs=0 V

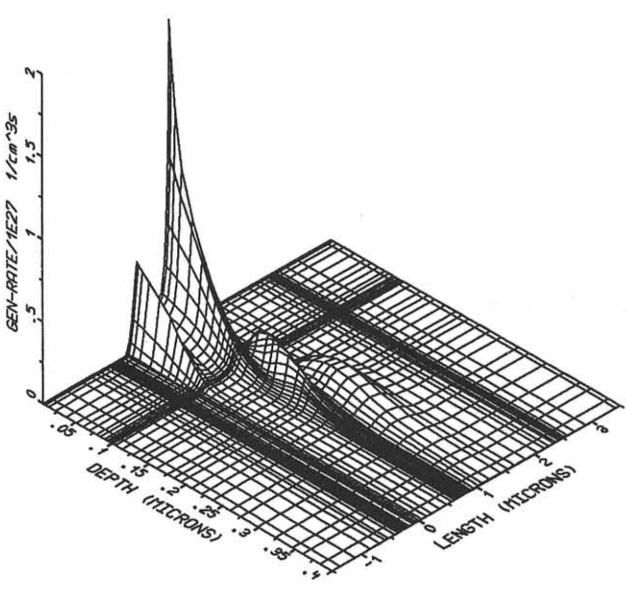


Fig. 3 Avalanche generation rate for Vgs≈V_T

Under pinch-off condition two peaks at the gate edges are observed, the peak at the drain side of the gate being significantly larger (Fig. 3). These simulation results are in good qualitative agreement with observations of Yamamoto et al.[10] on epitaxial power MESFETs.

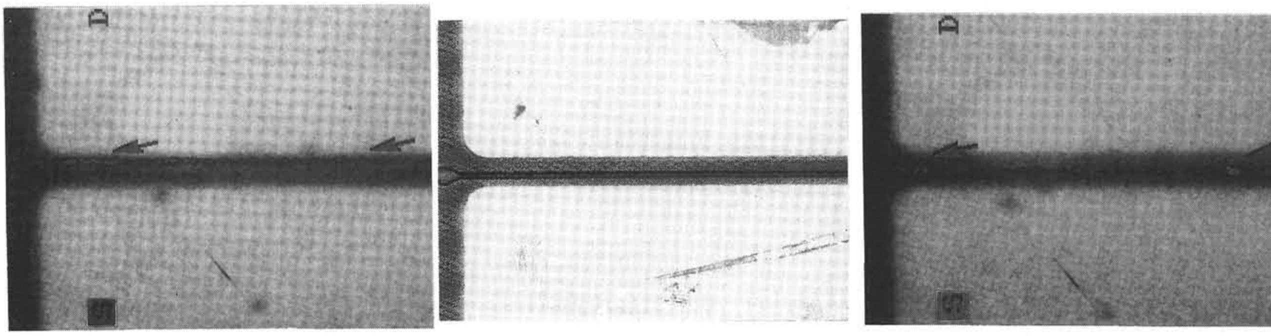
The physical origin of these simulation results can be explained by consideration of equation (1). In the case of open channel breakdown (V_{gs} = 0 V) an appreciable density of electrons are accelerated by the moderate electric field of the n^+-channel implant interface. In comparison, the density of holes and electrons accelerated onto and away from the gate contact is negligible. Thus the J_n in the $\alpha_n \cdot |J_n|$ product in (1) determines the breakdown location at the n^+-channel implant interface for V_{gs} = 0 V. For subthreshold breakdown ($V_{gs} \leq V_T$) however, the density of electrons (J_n) flowing to the drain is negligible. Furthermore, for large negative gate bias it has been shown that the electric field about the edges of the gate contact is dominant in the device[2]. It is proposed that the impact ionisation is initiated by the relatively low density of electrons and holes which enter the high electric field region about the gate edges. The created electron-hole pairs go on to cause secondary ionisation. This means that for $V_{gs} \leq V_T$ the α_n, α_p values in equation (1) determine the breakdown location at the edges of the gate contact.

At high drain bias the density of generated electron-hole pairs will be high enough to allow direct radiative interband recombination[7]. The recombination rate of carriers due to this mechanism is directly proportional to the concentration of electron-hole pairs generated by impact ionisation. Therefore, a measurement of the light emitted from a device can be directly compared to the carrier generation rate obtained by the simulation results.

5. EMISSION MICROSCOPY

The light emission of MESFETs at breakdown conditions has been investigated by emission microscopy using Hamamatsu's Hot Electron Analyzer as described by Boit et al.[8]. This setup allows the accurate superposition of the reflection and the emission image with the submicron resolution necessary in this study. For the emission detection a band pass filter at 800 nm, corresponding to 1.55 eV, has been used in conjunction with a S1 cathode.

The emission microscopy results obtained on the self-aligned MESFETs investigated in this study are given in Fig. 4. For V_{gs} = 0V the light emission occurs near to, but not directly at the edge of the drain contact of the FET (Fig. 3a). This is exactly the region of the edge of the n^+ implant (distance from



(a) (b) (c)

Fig. 4 Light emission from the device shown in Fig. 1 at bias conditions (a) Vgs = 0 V, (c) Vgs ≈ V_T. The arrows indicate regions of highest emission intensity. The microphotograph (b) shows the gate location.

drain metal = 0.4 µm, see Fig. 1), which also has been confirmed by measuring the light emission of FETs with different separations between drain contact and n^+ implant. Changing the gate voltage to more negative values, the light emission reduces drastically until pinch-off condition is reached ($V_{gs} \approx V_T$) when emission begins at the drain edge of the gate (Fig. 4c). This behaviour correlates exactly to the gate bias dependence of the breakdown location as predicted by simulation.

Additional simulations show that the shape and height of the impact ionization peak depends strongly on the surface state density and on the abruptness of the channel to n^+ interface as has been observed experimentally for different passivation schemes and contact implants.

6. CONCLUSION

Using the device simulator MINIMOS the breakdown behaviour of a self-aligned power MESFET due to impact ionisation could be studied by self consistent two-dimensional numerical calculations. All structural data of the device, including the four-fold implantation scheme, were taken into account. The location where breakdown occurs has been found to be strongly gate bias dependent:

(A) For V_{gs} = 0 V (open channel condition) a peak in the carrier generation rate occurs at the interface between the channel and the n^+ implant near the drain.

(B) For $V_{gs} \leq V_T$ (subthreshold condition) the generation rate of electron hole pairs is highest at the gate edges.

The position of light emission and its gate-bias dependence corresponds exactly to the peaks in the impact ionisation rates obtained by simulation. Therefore it can be concluded that the MINIMOS simulator and light emission microscopy are very helpful tools for optimizing GaAs power FETs.

7. ACKNOWLEDGEMENTS

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