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High-Speed Planar InP/InGaAs Avalanche Photodiodes with Optimized Electric Field Profile

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We confirmed in experiments that the avalanche in InGaAs diminishes the gain-bandwidth (GB) product of the InP/InGaAs avalanche photodiode (APD). GB product measurements agreed well with the calculated GB products, taking into consideration the ionization in InP and InGaAs. By suppressing the ternary layer avalanche and heterointerface pileup, we fabricated a high-performance APD with a large GB product of 95 GHz and a wide bandwidth of 8.5 GHz.

1. INTRODUCTION

InP/InGaAs avalanche photodiodes (APDs) are key devices in optical communication systems in the 1.55-μm wavelength range. Gain-bandwidth (GB) products must be improved to fabricate high-speed APDs[1, 2] operating at about 10 Gbit/s. Previous studies have shown that the avalanche in the InGaAs absorption layer would prevent generation of a large GB product[3, 4, 5]. However, to date there has been little rigorous discussion comparing experiments and theory. We have calculated the effect of the avalanche in InGaAs on the GB product, taking into consideration the ionization in InP and InGaAs, and have shown the GB product to be a function of InP multiplication layer thickness[6]. In this work, we studied the effect of the avalanche in the ternary layer. GB product measurements deteriorated as the electric field in the InGaAs layer rose and agreed well with calculations. We confirmed that the avalanche in InGaAs diminishes the GB product.

If the electric field in InGaAs is decreased to suppress the avalanche in the ternary layer, the 3-dB bandwidth deteriorates due to hole trapping[7] at the heterointerface. There is a tradeoff between the GB product and the 3-dB bandwidth for the electric field at the heterointerface.

In the optimized diode, suppressing the ternary layer avalanche and heterointerface pileup yield a high-performance APD having both a large GB product and a wide 3-dB bandwidth.

2. CALCULATION MODEL

Figure 1 shows the electric field of the calculated InP/InGaAs APD with a low(n^-)-high(n^+)-low(n^-) doping profile. The n^--InGaAs absorption layer thickness has been selected to be 1.5 μm to get a high-speed response and a quantum efficiency of 70%. The n^+-InP layer has been intended to decrease the electric field in the InGaAs layer and its thickness has been ignored. The electric field of the InP multiplication layer and the InGaAs absorption layer have been

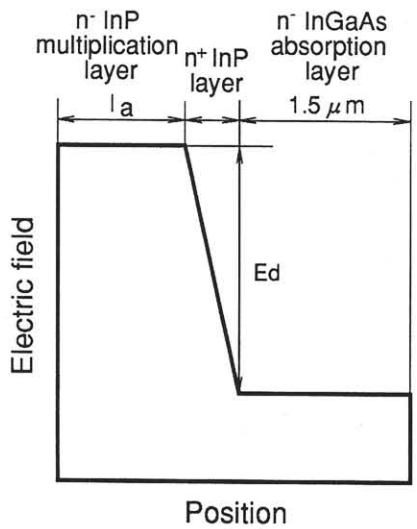

Fig. 1 Electric field profile model of calculated APD.

assumed constant. These electric fields are determined by the InP multiplication layer thickness, la, and a difference of the electric field value between the absorption layer and the multiplication layer, Ed. The GB product has been calculated changing la and Ed by considering ionization both in InP and InGaAs.

3. FABRICATION

Figure 2 shows each layer of the fabricated APD. According to our calculation, the n^--InGaAs absorption layer ($n = 2 \times 10^{15}$ cm^{-3}) was 1.5 μm thick. The n^+-InP layer ($n > 5 \times 10^{17}$ cm^{-3}) causing of decreasing the electric field in the InGaAs layer was thinned to about 600 Å to reduce the carrier transit time. Ed is determined by the total charge in this layer. Therefore, Ed can be selected to be 3.5×10^5 V/cm, 4.5×10^5 V/cm, and 5.5×10^5 V/cm by changing the thickness and carrier concentration in this layer. The n^--InP window layer ($n = 2 \times 10^{15}$ cm^{-3}) having 1.5 μm thick was grown at the top. To make a

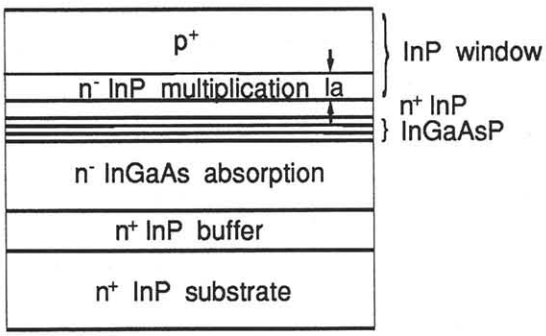

Fig. 2 APD epitaxial structures.

planar junction, we formed a p^+ region and a guard ring by selective Cd diffusion and Be ion implantation. The n^--InP multiplication layer thickness was controlled by the depth of Cd diffusion. Three undoped InGaAsP layers were introduced in the heterointerface to prevent hole pileup. To prevent increasing the carrier transit time for adding these layers, each layer was thinned to 500 Å. The band gaps were, from the top, 1.10 eV, 0.95 eV, and 0.80 eV.

4. RESULT AND DISCUSSION

Figure 3 shows the dark current and multiplication factor versus the bias voltage (I-V and M-V characteristics) of the fabricated APD. The breakdown voltage was less than 30 V because of the thin n^+-InP layer reducing

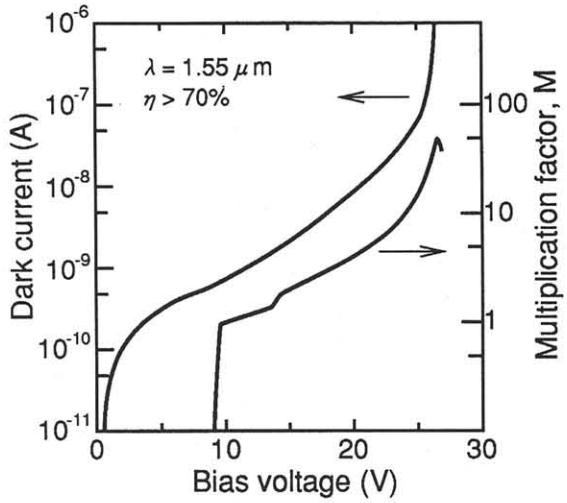

Fig. 3 Dark current and multiplication factor versus bias voltage. A step at about 14 V of M-V characteristic shows a voltage when the depletion region reaches the absorption layers.

the electric field. The dark current was about 40 nA at a 90% breakdown voltage. The origin of multiplication (M = 1) was determined by compared with the calculated M-V characteristic. The maximum multiplication factor was 50 at the breakdown voltage. Quantum efficiency was more than 70% at a wavelength of 1.55 μm and agreed with calculations.

The M-V characteristic was observed increasing a step at about 14 V. This voltage indicates when the depletion region under the pn junction reaches the InGaAs absorption layer. The multiplication layer thicknesses were calculated using this voltage for each APD chips.

Figure 4 shows GB product as a function of the multiplication layer thickness at each Ed. The calculated GB products (solid lines) deteriorate with increasing avalanche buildup time in the wider la region. In the narrower la region, the overall electric field in the diode becomes high, and the GB product is degraded due to the onset of the avalanche in the ternary layer. The optimum la exists to obtain the maximum GB product. The maximum GB product can increase as Ed increases. GB product measurements (data points) agreed well with the calculations. We confirmed that the ionization in InGaAs diminishes the GB product.

Figure 5 shows the 3-dB bandwidth versus multiplication factor at a Ed of 5.5×10^5 V/cm and a la of 0.19 μm. By optimizing the electric field profile to suppress the avalanche in the ternary layer, we obtained a large GB product of 95 GHz in a high multiplication region of more than 10. A wide bandwidth ceiling of 8.5 GHz determined by

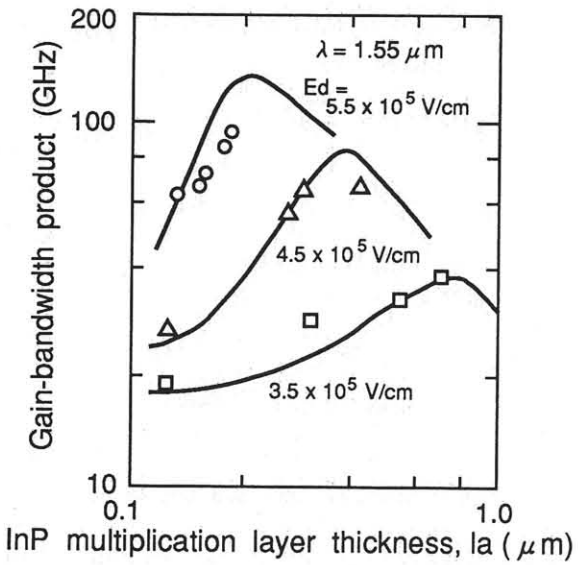

Fig. 4 Gain-bandwidth product versus InP multiplication layer thickness. The solid lines are calculated GB products and the data points are measured GB products.

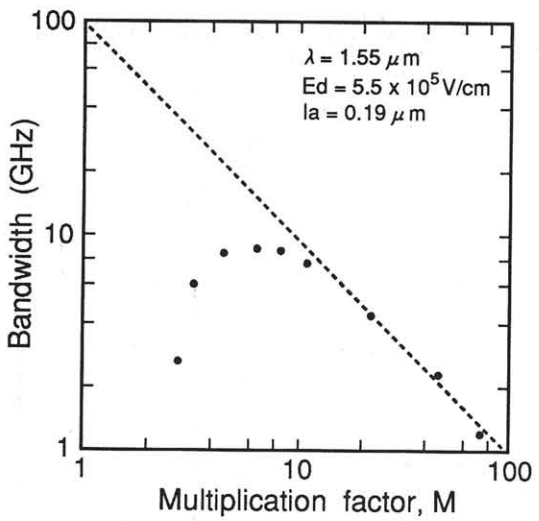

Fig. 5 Bandwidth versus multiplication factor. The dashed line shows a GB product of 80 GHz.

the transit time was obtained by suppressing hole pileup.

5. CONCLUSION

We confirmed that the gain-bandwidth product of InP/InGaAs APDs deteriorates due to ionization in the InGaAs. Optimizing the electric field profile and heterointerface produced an InP/InGaAs APD with a large gain-bandwidth product of 95 GHz and a wide bandwidth of 8.5 GHz.

6. REFERENCES

1) J. C. Campbell, W. T. Tsang, G. J. Qua, and J. E. Bowers, Appl. Phys. Lett. 51(1987) 1454.
2) L. E. Tarof, IEEE Photonics Technol. Lett. 2(1990) 643.
3) M. Kobayashi, H. Machida, T. Shirai, Y. Kishi, N.Takagi, and T. Kaneda, Technical Digest of OFC'87(1987) paper MJ 3.
4) J. N. Hollenhorst, D. T. Ekholm, J. M. Geary, V. D. Mattera, Jr., and R. Pawelek, SPIE Proc., 995(1988) Conf. on High Frequency Analog Commun., MA Sept.
5) H. C. Hsieh and W. Sargeant, IEEE J. Quantum Electron., 25(1989) 2027.
6) H. Kuwatsuka, Y. Kito, M. Ito, and T. Mikawa, Technical Digest of ECOC'90 (1990) 385.
7) J. C. Campbell, B. C. Johnson, G. J. Qua, and W. T. Tsang, J. Lightwave Technol., 7(1989) 778.