Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials, Yokohama, 1991, pp. 411-413

Effect of Si Interlayers on Heteroepitaxial Films of GaAs/Si/GaAs and GaAs/Si/GaAs/Si System

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A multichamber MBE system has been used to deposit thin Si interlayers in GaAs films grown on (001) Si substrates tilted 2° toward the [110] direction to control the threading dislocation motion. The maximum Si thickness is ~ 1 nm for no defect generation in Si-inserted GaAs films homoepitaxially grown on (001) GaAs substrates. The following experiment clearly demonstrates that some 60°-type threading dislocations change their running directions at every depth where ~ 1 nm thick Si interlayers are inserted into GaAs films grown on the above Si substrates.

1. INTRODUCTION

We have recently reported[1] that the threading dislocations generated by GaAs on Si change their moving directions at the insertion region of very thin Si interlayers, resulting in a dislocation density reduction at the film surface. This was considered to be due to a blocking effect of the Si interlayer for dislocation propagation in GaAs caused by the strong covalent bonding of Si-Si. However, the above-mentioned experiments were performed in a conventional III-V MBE chamber using Si effusion from a Knudsen-cell. It was thus rather difficult to exactly control and to freely change the deposited thickness of the Si interlayers. To overcome these problems, we constructed a multichamber MBE system in which the alternate growth of III-V and Si can be performed with ease. By using this multichamber, we studied in detail the effect of Si interlayers on the threading dislocation motion in GaAs on Si.

2. EXPERIMENTS

Both GaAs and Si growth was performed in a newly constructed multi-chamber MBE system. Samples were kept under an ultrahigh vacuum during the transfer through the exchange chamber from the III-V (or Si) to the Si (or III-V) MBE chamber. By using this system, two different experiments for thin Si interlayer deposition were performed as follows.

First, we grew Si interlayers with various thicknesses in homoepitaxial GaAs films to obtain the maximum Si interlayer thickness for which no defects are generated in Si-deposited GaAs films. GaAs layers were grown on semi-insulating GaAs (001) wafers at a rate of 1 ML/s at 600 °C. Just after an adequate GaAs growth, the samples were transferred into the Si MBE chamber where Si was deposited at a rate of 1 ML/s at 250 °C by electron beam deposition. After growing Si of various thicknesses from 0.5 to 5 nm, the samples were transferred back into the III-V MBE chamber and GaAs growth was again undertaken to a total thickness of ~ 3 μm.

Next, GaAs heteroepitaxial growth experiments having Si interlayers were carried out using Si (001) wafers inclined 2° toward the [110] direction. After surface-cleaning of the Si substrates (900 °C for 15 min), 10 ML AlAs layers were first grown at 500 °C by an alternating source supply method. Then, the GaAs and Si growth was followed with the same procedure as described above.

3. GaAs/Si/GaAs SUBSTRATE SYSTEM

Figure 1 shows an XTEM micrograph of a GaAs homoepitaxial film having both ~ 0.5 and ~ 1 nm thick Si interlayers in different depths as indicated in the figure. As clearly seen from the micrograph, no defect generation is observed in the whole GaAs film, nor near the GaAs/Si interface regions where two thin Si layers were deposited. Figure 2 shows a high-resolution XTEM micrograph

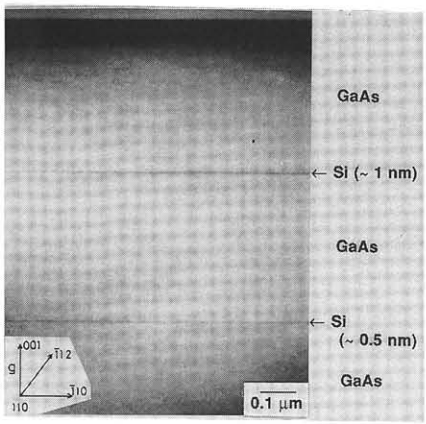

Fig. 1 An XTEM micrograph of a homoepitaxial GaAs film having ~ 0.5 and ~ 1 nm thick Si interlayers.

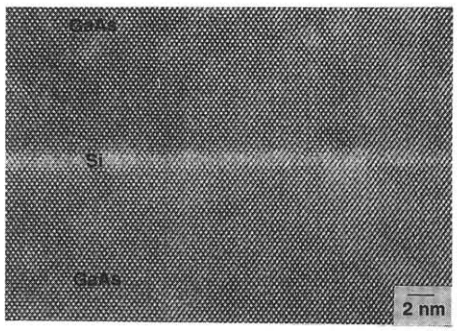

Fig. 2 A high-resolution XTEM micrograph showing the GaAs/Si area having ~ 1 nm thick Si. [110] projection.

of the GaAs/Si area having ~ 1 nm thick Si shown in Fig. 1. Generation of neither dislocations nor antiphase domains (APD) is detected from the lattice image of the interface region between GaAs and Si, although a not very sharp interface is formed probably due to the early stages of three-dimensional growth[3]. This result shows that such a thin Si layer grows pseudomorphically on the (001) GaAs substrate.

However, crystal defects such as dislocations and APDs were severely created in GaAs films with Si layers thicker than ~ 1.5 nm. Figure 3 shows a homoepitaxial GaAs film having Si interlayers of five different thicknesses at different depths in the film as shown in the micrograph. From this result, we can distinctly see the generation of dislocations, stacking faults and APDs in every upper GaAs layer from the interface. Also, we note that their density increases with increasing Si thickness. It was confirmed by high-resolution TEM observations that these thin Si layers are highly defective[3] and misfit dislocations at both upper and lower interfaces between Si and GaAs are clearly generated with coexistence of edge-type and 60°-type dislocations. One example is shown in Fig. 4 for a micrograph taken for a region having a 4.6 nm thick Si layer.

From these results, the critical thickness of Si for

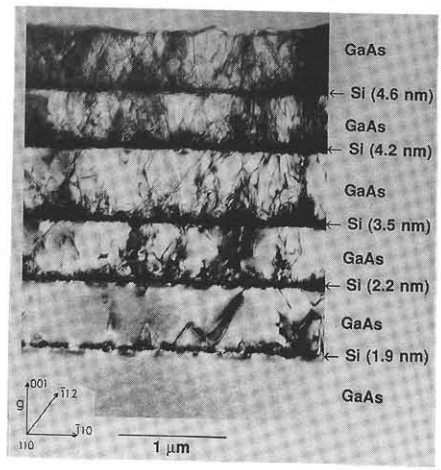

Fig. 3 An XTEM micrograph of a homoepitaxial GaAs film having Si interlayers of five different thicknesses as shown in the micrograph.

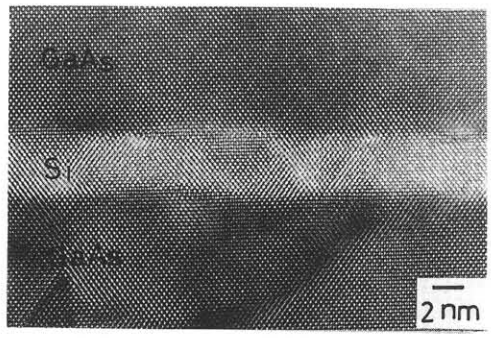

Fig. 4 A high-resolution XTEM micrograph showing the GaAs/Si area having 4.6 nm thick Si,[110] projection.

defect generation in a GaAs film with such an inserted Si layer was determined to be between ~ 1 and ~ 1.5 nm.

4. GaAs/Si/GaAs/Si SUBSTRATE SYSTEM

On the basis of section 3 results, we deposited a ~ 1 nm thick Si layer at various depths in GaAs films grown on Si substrates to control threading dislocation motion in GaAs. Figure 5 shows the distinct effect of Si layers inserted at different depths of 0.5, 1 and 2 μm above the interface between GaAs and Si on the dislocation behavior. We can clearly see that some dislocations running along the <110> and <211> directions on the {111} planes inclined from the (001) substrate surface change their running directions, at the exact positions where thin Si was inserted, into the ±[$\bar{1}$ 10] direction parallel to the interface.

We can also clearly see the effect of Si layers in the result shown in Figs. 6 and 7. The sample in these figures shows three Si interlayers ~ 1 nm thick inserted separately by 25 nm at a depth of ~ 500 nm from the interface. Overall, the dislocations threading over the Si layers in Fig. 6 appear to be reduced,

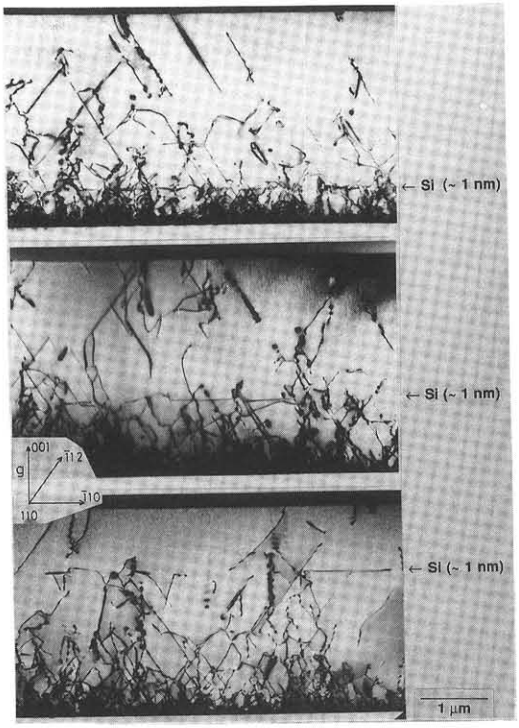

Fig. 5 XTEM micrographs of heteroepitaxial GaAs films having ~ 1 nm thick Si interlayers at different depths grown on Si.

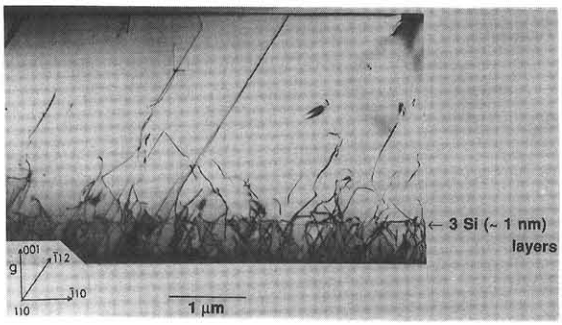

Fig. 6 An XTEM micrograph of a heteroepitaxial GaAs film having three Si interlayers separately inserted by 25 nm at a depth of 500 nm from the interface.

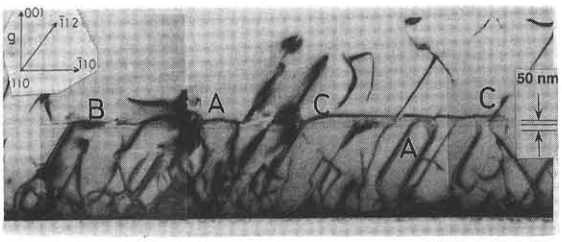

Fig. 7 An enlarged XTEM micrograph near the Si inserted region of a Fig. 6 sample.

compared to the dislocations in the sample including one Si layer at the same depth of 0.5 μm in Fig. 5. Figure 7 is an enlarged micrograph near the Si inserted region. We can categorize the dislocations affected at the Si layers into the following three classes of A, B and C as indicated in the figure. (a) Dislocations A alter the moving direction, for example, from [$\bar{1}$12] to [$\bar{1}$10] at one inserted position of three layers and go back again into the substrate side. (b) Dislocations B terminate at the interlayer probably due to the alteration of the moving direction from [$\bar{1}$12] to [110] normal to the film surface. (c) Dislocations C change their directions at the interlayers but again thread toward the surface. Also, there are some dislocations threading with no effect of Si layers on the moving direction.

Thus, as shown above, the thin Si interlayer has an excellent ability to block threading dislocation propagation from the GaAs/Si interface to the surface. An interesting point in the present experiment is that only a few Si monolayers are effective in dislocation blocking. This is in contrast to the experiment of the so called strained-layer superlattice insertion, where generally, 10 periods of two ~ 10 nm thick layers are used. This might be caused by two different effects. One effect is due to a 4 % mismatch stress between GaAs and Si. As stated in section 3, a Si interlayer grows pseudomorphically on a GaAs substrate. Therefore, an induced-strain field from the interface must able to sweep out dislocations along the direction parallel to the interlayers. Another effect comes from the different "hardness" between GaAs and Si as discussed in a previous paper[1].

5. CONCLUSION

First, the maximum Si thickness was determined to be ~1 nm for generation of no defects in the GaAs/Si/GaAs substrate system. A high density of defects such as APDs and threading dislocations was generated in the top GaAs film, if the insertion thickness of Si exceeded ~ 1.5 nm. On the basis of the above result, we inserted ~ 1 nm thick Si layers into GaAs films for a GaAs/Si/GaAs/Si substrate. Some 60°-type dislocations were clearly bent into the direction parallel to the inserted layer and/or retured to the substrate side at the Si inserted position. However, Si insertion methods must be improved to further suppress the threading dislocation density to get to the film surface.

REFERENCES

1) A.Hashimoto, N.Sugiyama and M.Tamura, Jpn. J. Appl. Phys. 30 (1991) L447.
2) D.K.Biegelsen, R.D.Bringans, J.E.Northrup and L.E.Swartz, Appl. Phys. Lett., 57 (1990) 2419.
3) Z.Liliental-Weber and R.P.Mariella Jr, Mater. Res. Soc. Symp. Proc., 148 (1989) 241.