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Control of GaAs and InGaAs Insulator-Semiconductor and Metal-Semiconductor Interfaces by Ultrathin MBE Si Layers

Masamichi Akazawa, Hirotatsu Ishii and Hideki Hasegawa
Department of Electrical Engineering and Research Center for Interface Quantum Electronics , Hokkaido University,
North 13, West 8, Sapporo 060, Japan
TELEFAX 011-757-1165 PHONE 011-757-1163

Removal or control of Fermi level pinning is attempted by using an ultrathin MBE Si interface control layer (Si ICL) for insulator-semiconductor and metal-semiconductor of GaAs and InGaAs.

For successful removal of Fermi level pinning at I-S interface, the Si ICL should maintain an ordered pseudomorphic structure. The optimum thickness of the Si ICL is about 10Å. Pinning at the air exposed surfaces can be removed by combining an HF surface treatment with the Si ICL technique. The Si ICL technique is promising for controlling barrier heights at M-S interfaces.

1.Introduction

Surfaces of compound semiconductors are generally characterized by presence of high densities of surface states which cause uncontrollable strong "pinning" of the surface Fermi level. However, as the device dimension is scaled down to the nanometer quantum regime, removal of "pinning" or control of pinning position at surfaces and interfaces becomes obviously more and more important.

We have recently shown that use of an ultrathin MBE-Si interface control layer (ICL) on MBE grown clean surfaces of GaAs and InGaAs drastically reduces the Fermi level pinning[1-3], resulting in improved performance and stability of MISFETs and PCDs[4,5].

In this paper, the fundamental unpinning mechanism in the Si ICL technique is investigated. Then, the Si ICL technique is extended to air-exposed surfaces and metal-semiconductor (M-S) interfaces on GaAs and InGaAs. It is found that Si ICL is useful to remove pinning at I-S interfaces and to control the pinning position at M-S interfaces.

2.Experimental

Preparation sequence and structure of the samples are shown in Fig.1.

Three types of samples having Si ICLs are prepared, i.e., (a) I-S samples by UHV processing (b) I-S samples including air-exposure and (c) M-S samples.

GaAs and InGaAs layers were prepared by MBE. For the air-exposed I-S samples, the surfaces were subjected to various surface treatments including chemical etching, thermal cleaning under As overpressure and HF treatment. The ultrathin Si ICL(10-80Å) was grown by MBE. For I-S interfaces, thick outer SiO_2 layer was deposited by a photo-CVD process using SiH_4, N_2O and an ArF excimer laser. For M-S interfaces, Al was deposited.

At each step of sample fabrication, surface was investigated by in-situ RHEED and XPS technique. For electrical characterization, capacitance-voltage (C-V) and current-voltage (I-V) measurement were carried out.

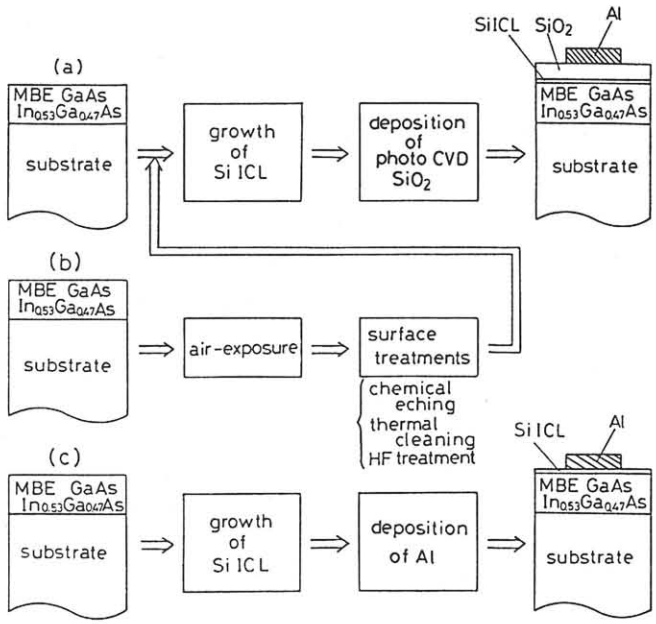

Fig.1 Preparation sequences and structures of the samples. (a) UHV processed I-S sample, (b) air-exposed I-S sample, (c)M-S sample

3. Experimental Results

3.1 Fermi level movement in samples by UHV processing

Figure 2 shows Fermi level position vs. Si ICL coverage investigated by in-situ XPS. Fermi level shifts towards the conduction band edge with the increase of Si coverage, for both n and p type samples. This result indicates that formation of Si ICL only does not remove Fermi level pinning caused by surface states.

Up to the Si ICL thickness of about 10Å, the RHEED pattern showed (3x1) surface reconstruction for Si/GaAs and (3x3) reconstruction for Si/InGaAs. Beyond this thickness, the RHEED intensity rapidly decreased and the pattern finally became halo.

The pinning of the Fermi level which existed after Si ICL formation as seen in Fig.2, was removed after deposition of the outer SiO_2 layer and annealing. However, degree of its removal was found to depend critically on the Si ICL thickness. Figure 3 plots the minimum value of the interface state density measured by the C-V method against the thickness of the Si ICL for InGaAs

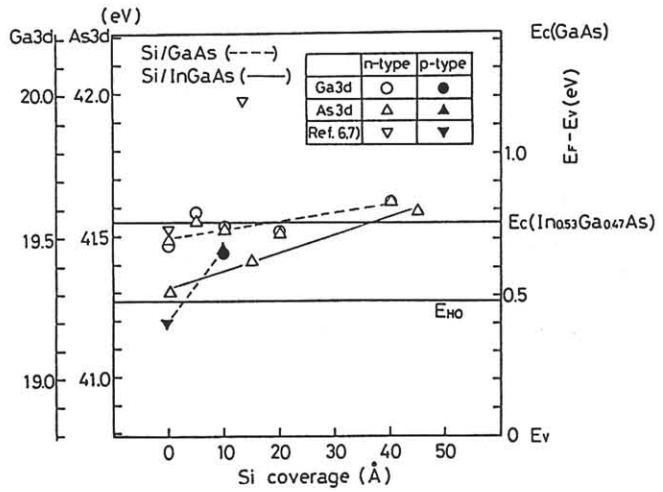

Fig.2 E_F movement vs. Si coverage

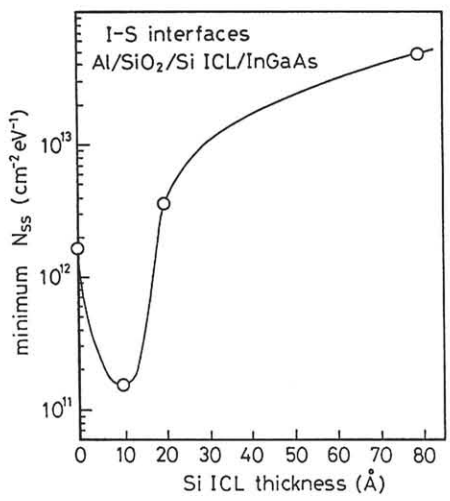

Fig.3 Minimum N_{ss} vs. Si ICL thickness

MIS structures. The interface state density (N_{ss}) became smallest when the thickness of Si ICL was 10Å.

3.2 Unpinning of Fermi level in air-exposed I-S sample

The applicability of the Si ICL technique using the UHV processing to device fabrication is very much limited, since air-exposure of the semiconductor surface is not allowed throughout the whole processing. To overcome this difficulty, various surface treatments were tried as shown in Fig.1(b). Chemical etching was done using $H_3PO_4:H_2O_2:H_2O=1:1:38$ solution. Thermal cleaning was carried out in the MBE chamber under As overpressure. In HF treatment, InGaAs was immersed after chemical etching into an HF solution under N_2 atmosphere. Interface state density (N_{ss}) distributions of the SiO_2/Si ICL/InGaAs MIS structure based on Terman method, are summarized in Fig.4. The HF treatment was most effective for N_{ss} reduction, giving N_{ss} of $8.6\times10^{10}cm^{-2}eV^{-1}$, which is lower than that by UHV process. On the other hand, chemical etching and thermal cleaning led to high N_{ss}.

A detailed XPS study indicated that the HF treatment removed efficiently the Ga_2O_3 component of the surface oxide leaving As_2O_3 and elemental As components. The subsequent deposition of the Si ICL, then removes these As components almost completely, leaving an oxide-free and stoichiometric surface. On the other hand, the thermal cleaning removed oxide, but deteriorated the stoichiometory very much.

3.3 Control of Fermi level in M-S sample

An attempt was also made to control the Schottky barrier height (SBH) of Al/GaAs interface using Si ICL. Figure 5(a) shows

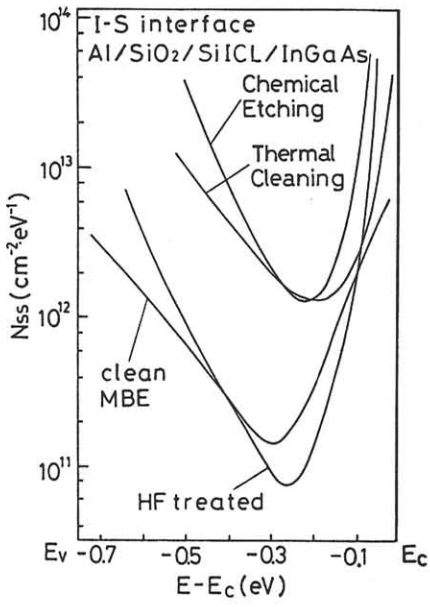

Fig.4 N_{ss} distribution at I-S interface with Si ICL

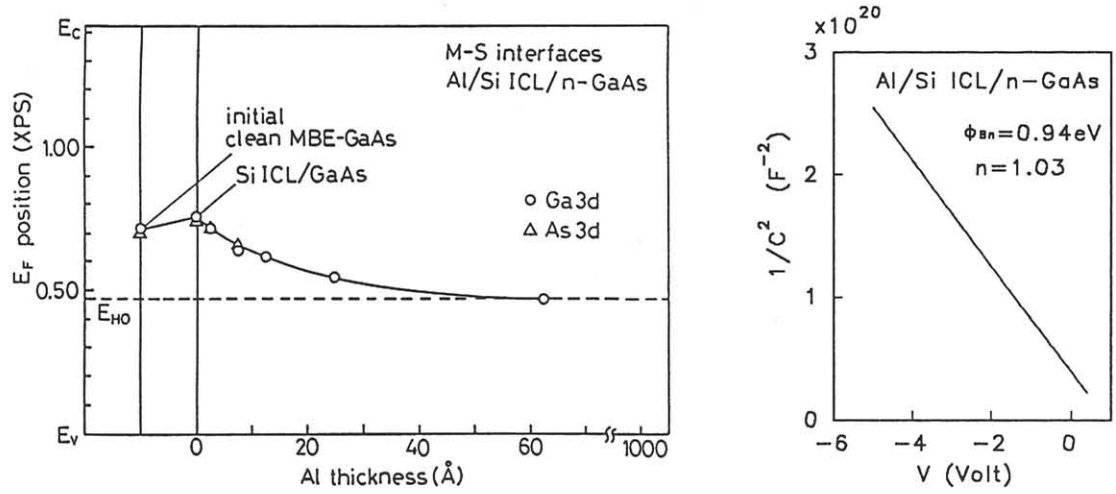

Fig.5 (a) Fermi level movement at M-S interface with Si ICL and (b) C^{-2}-V plot of the Al/Si ICL/GaAs sample

Fermi level movement during formation of Al/Si ICL/GaAs interface by in-situ XPS study. It is seen that the Fermi level position is lowered by interface formation, indicating an increase of the SBH for the n-type sample. This was confirmed by the C^{-2}-V plot of completed Al/Si ICL/GaAs sample shown in Fig.5(b). C-V and I-V results showed SBH of 0.94eV with n=1.03. C-V curves showed no frequency dispersion, indicating excellent interface property. On the other hand, Al/clean MBE n-GaAs Schottky barrier exhibited low barrier heights (0.6-0.7eV) with larger ideality factors.

4.Discussion

The Fermi level pinning at the Si ICL/GaAs and the Si ICL/InGaAs surfaces in Fig.1 can be explained either by formation of new surface states bands corresponding to the observed (3x1) and (3x3) surface reconstruction or by doping of Si into the GaAs and InGaAs surfaces. A further study is necessary to clarify this point.

The existence of the optimum Si ICL thickness for I-S interfaces strongly indicates the importance of maintaining an ordered pseudomorphic surface for successful removal of pinning. The success of unpinning on the air-exposed surfaces shows the importance of maintaining an oxide-free stoichiometric surface. Both of these features are consistent with the disorder-induced gap state (DIGS) model[8] for Fermi Level pinning.

The shift of the Fermi level position in the M-S interface can be understood by formation of an semiconductor like interface layer with shallow acceptor impurities (Ga) and a reduced DIGS density at the Si/GaAs interface. Such a technique for SBH enhancement appears to be very promising for device applications.

5. Conclusion

(1) For successful removal of Fermi level pinning at I-S interface, the Si ICL should maintain an ordered pseudomorphic structure. The optimum thickness of the Si ICL is about 10Å.
(2) Pinning at the air exposed surfaces can be removed by combining an HF surface treatment with the Si ICL technique.
(3) The Si ICL technique is promising for controlling barrier heights at M-S interfaces.

Acknowledgment

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References

1)H. Hasegawa et al: Jpn. J. Appl. Phys. Vol.27, No.12, L2265
2)H. Hasegawa et al: J. Vac. Sci. Techonol **B7**, 870(1989).
3)H. Hasegawa et al: J. Vac. Sci. Techonol **B8**, 867(1990).
4)M.Akazawa et al:Jpn. J. Appl. Phys. Vol.28, No.11, L2095
5)K.Iizuka et al.:Proc. of 1989 Int. Symp. GaAs and Related Comp.(1989,Karuisawa),743.
6)R.W.Grant and J.R.Waldrop: J. Vac. Sci. Techonol **B5**, 1015 (1987).
7)J.R.Waldrop and R.W.Grant: Appl. Phys. Lett. **52**(21), 1794 (1988)
8)H.Hasegawa and H.Ohno:J. Vac. Sci. Technol.**B4**,1130(1986).