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Symmetric P-n-P InAlAs/InGaAs Double Heterojunction Bipolar Transistor's Fabricated with Si-ion Implantation

Atsushi Nakagawa , and Kaoru Inoue
Semiconductor Research Center, Matsushita Electric Industrial Co., LTD
3-15, Yagumo-Nakamati, Moriguti, Osaka, 570 Japan

A symmetric double-heterojunction bipolar transistor (DHBT) epitaxially grown on a semi-insulating substrate not only has obvious advantages for I^2L and ECL circuits, but it can also improve high-speed performance in the emitter-down mode[1]. Recent analysis suggests P-n-p HBT's have the potential for performance approaching that of N-p-n HBT's [2]. We expect the InGaAs / InAlAs system, lattice-matched to InP, to be very promising for the symmetric P-n-P DHBT because **1)** the large conduction-band offset, approximately 0.5eV, improves the blocking of hole injection from the external portion of the emitter in the emitter-down mode,(compared with a symmetric GaAs/AlGaAs DHBT), **2)** the turn-on voltage is smaller than the N-p-n GaAs / AlGaAs HBT,which can make the power dissipation very low, **3)** the large electron mobility in n-InGaAs can make the base resistance very low. A symmetric P-n-P InGaAs/InAlAs DHBT has not yet been reported, although it is expected to be attractive for I^2L and ECL circuits with low power dissipation.

In this letter we report the first demonstration of symmetric P-n-P InGaAs/InAlAs DHBT's which can operate in both the emitter-up mode and the emitter-down mode. An abrupt heterojunction causes a spike in the conduction band (or the valence band) which reduces the collection of electrons (or holes) at the base-collector junction, as has been suggested by Kroemer[1]. To overcome this effect in case of the symmetric P-n-P InGaAs/InAlAs DHBT's two thin p-InGaAs layers are added in the base next to both the collector and the emitter; a similar technique was reported for N-p-N DHBT's [3],[4].

The layer structure used for the DHBT's and the device structure is shown in Fig.1. The epitaxial layer structure was grown by Molecular Beam Epitaxy (MBE) on a semi-insulating InP substrate at 490°C. The structure consists of an undoped $In_{0.52}Al_{0.48}As$ buffer (0.3 μm thick), a Be-doped $In_{0.53}Ga_{0.47}As$ subcollector layer ($4x10^{19}/cm^3$, 0.3 μm thick), a Be-doped $In_{0.52}Al_{0.48}As$ collector layer ($1.2x10^{17}/cm^3$, 0.3 μm thick), a Si-doped $In_{0.53}Ga_{0.47}As$ base layer ($1.8x10^{18}/cm^3$, 0.07 μm thick),a Be-doped $In_{0.52}Al_{0.48}As$ emitter layer ($1.2x10^{17}/cm^3$, 0.3 μm thick), and a Be-doped $In_{0.53}Ga_{0.47}As$ contact layer ($4x10^{19}/cm^3$, 0.1 μm thick). Two very thin Be-doped $In_{0.53}Ga_{0.47}As$ layers ($1.2x10^{17}/cm^3$, 0.04 μm thick) are added to both sides of the base. The contact and emitter layers were removed from the external base contact regions by wet chemical etching. Next, the external base regions were implanted with Si ions at an energy of 100keVand a dose of $1x10^{14}/cm^2$. The carriers were then activated by rapid thermal annealing (RTA) at 600°C for 10s. The subcollector layer was then exposed by mesa etching. Finally, base ohmic contacts were formed using AuGe/Ni/Au, and emitter and collector ohmic contacts were formed using Ti/Au.

Fig. 2(a)-(b) shows the typical collector-voltage characteristics for DHBT's in the emitter-up mode and the emitter-down mode. In devices with a $70x70\mu m^2$ emitter area , typical current gains of 20 and 14 were measured in the emitter-up mode and emitter-down mode, respectively. These current gains were lower than expected, but the structures were not optimized. This device gives a relatively small turn-on voltage of 0.62V at a collector current density of $200A/cm^2$, which is about a half that of a conventional N-p-n GaAs/AlGaAs HBT. The hole injection from the external emitter regions was suppressed by the factor of 10^{-3} ~10^{-4} because of the large difference in the turn-on voltage between the external base-emitter junctions and the internal ones. We expect to achieve further improvement by optimizing the material structure and modifying the fabrication technology.

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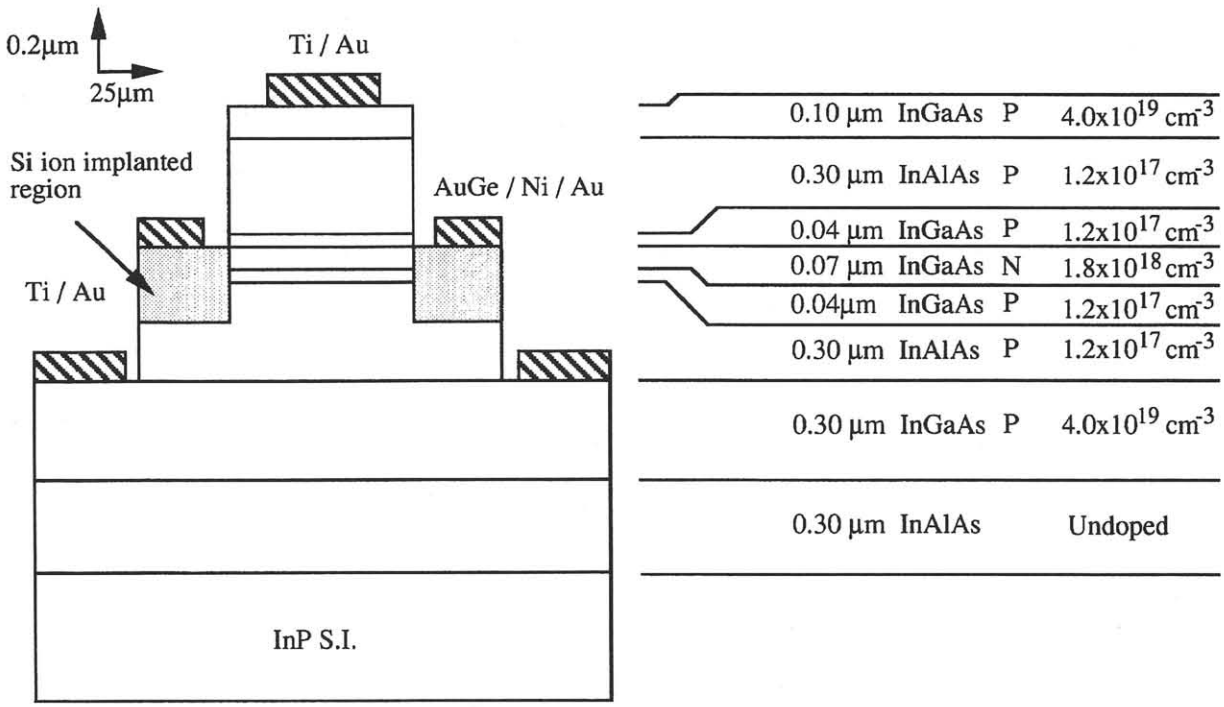
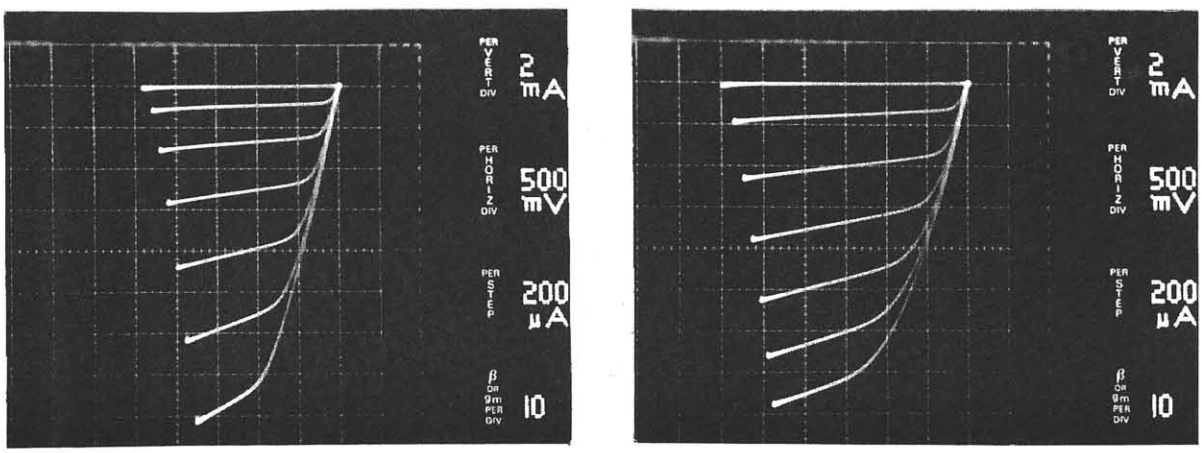


Fig. 1. Schematic cross section of the symmetric P-n-P InGaAs / InAlAs DHBT with an emitter area of 70 x 70 μm^2, and a collecror area of 140 x 170 μm^2 .



(a) (b)

Fig. 2. Typical collector current-voltage characteristics: (a) in the emitter-up mode; (b) in the emitter-down mode