

## A HEMT 64 K SRAM Grown by MOVPE

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We developed a low-pressure barrel reactor with a load capacity of twelve 3-inch wafers. A wafer rotation mechanism is employed to achieve extremely uniform epitaxial layers. The variations in both layer thickness and donor concentration of a Si-doped AlGaAs layer are less than  $\pm 1\%$  across a 3-inch wafer. The wafer-to-wafer variations among the twelve wafers are  $\pm 1.1\%$  for layer thickness and  $\pm 1.8\%$  for donor concentration. These figures are sufficiently small for LSI application.

Surface defects, or particles, on an epitaxial wafer degrade the performance and reliability of HEMT LSIs. To get an acceptable chip yield, surface defects should be reduced. We have succeeded in reducing the density of surface defects. The total density of particles larger than  $0.24 \mu\text{m}^2$  is  $8.0 \text{ cm}^{-2}$ .

The 1-nm spacer layer thickness was chosen to obtain a large enough two dimensional electron gas concentration and mobility. The typical electron mobility and sheet carrier concentration were  $6,200 \text{ cm}^2/\text{Vs}$  and  $1.0 \times 10^{12} \text{ cm}^{-2}$  at room temperature.

The reproducibility or run-to-run stability is a key factor for mass-production. Analyzing variations in the threshold voltages of the fabricated HEMTs, it was shown that the variations of epitaxial layer parameters less than  $\pm 1\%$  is maintained over depositions of 1,000 wafers.

We applied this MOVPE technology to a HEMT 64K SRAM. The gate length is  $0.6 \mu\text{m}$ . The standard deviations of threshold voltage are 11.6 mV for enhancement- and 12.0 mV for depletion-mode HEMTs. An excellent uniformity of 0.8 ps for a standard deviation of delay time was obtained at an average delay time of 22.6 ps/gate and a power dissipation of 0.8 mW/gate. A micrograph of the chip is shown in Figure 1. The chip size is  $7.4 \text{ mm} \times 6.5 \text{ mm}$  and the I/O interface is ECL-compatible. Figure 2 shows address input and data output waveforms. A typical address access time of 1.2 ns was obtained at a power dissipation of 5.9 W, including the I/O circuit.

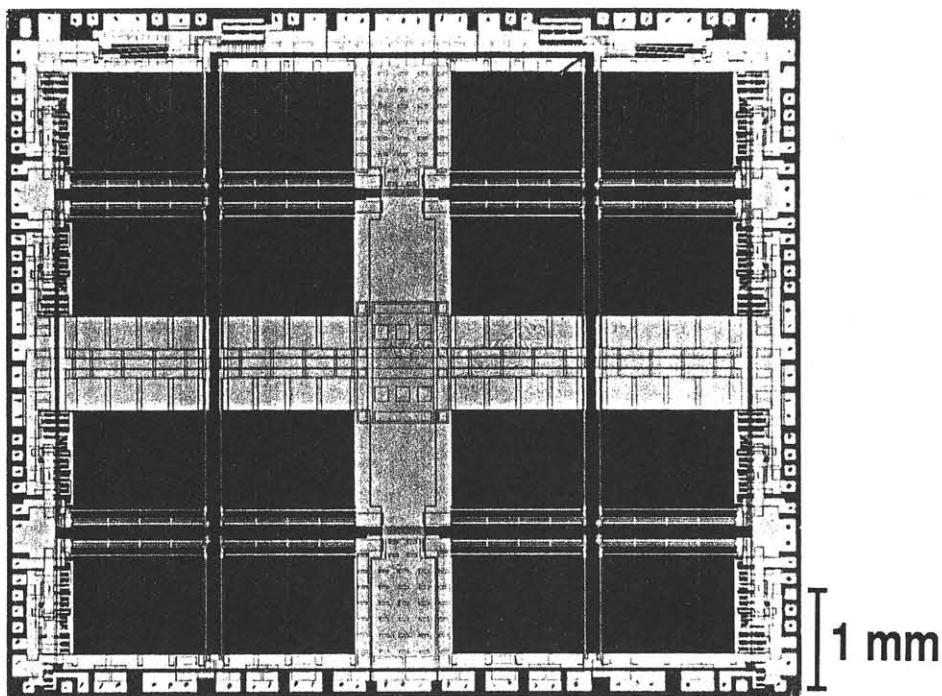


Figure 1 Micrograph of a HEMT 64K SRAM

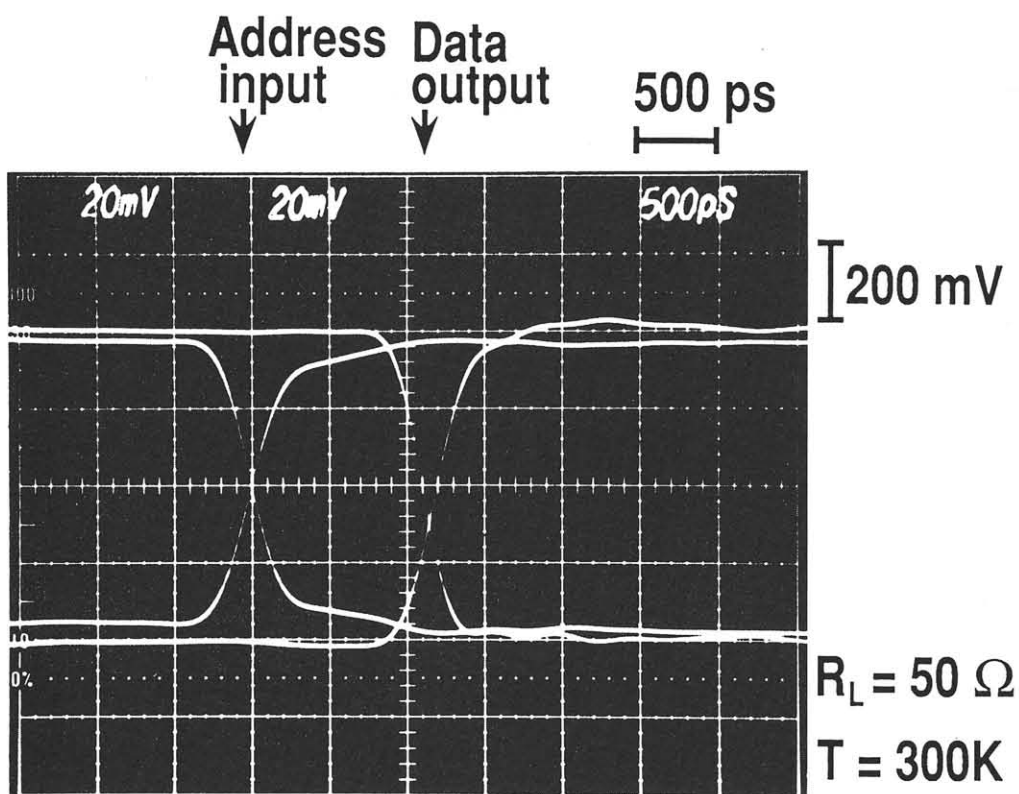


Figure 2 Address access time waveform