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Mechanism of Lowering TiW/Si Contact Resistivity by Post Annealing Process

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TiW/Si interfaces are characterized with various annealing temperatures. It is found that a thin silicide is found to be formed in the range of 600 ~ 700°C, and a thick silicide is formed above 750°C. The thick silicide breaks p/n junction, while the thin silicide does not break p/n junction and lowers p+contact resistance. The thin silicide identified by TEM as $(Ti_{1-x}W_x)Si_2$ is epitaxial on the silicon substrate, and the thickness is 4nm at 650°C.

1. Introduction

TiW is an effective barrier against alloy spiking, stress- and electro-migration in aluminum wiring systems, and it is widely used for Si ULSI applications. However, for the use on high speed switching devices, its contact resistance with p type diffusion layer is relatively high. Therefore silicides such as PtSi or $TiSi_2$ are preferred. Attempts for silicidation using W rich TiW were reported by several authors. [1, 2] They showed that disilicide of $(Ti_{1-x}W_x)Si_2$ is formed at the TiW/Si interface annealed at 725°C or higher. Recently, Onishi *et al.* reported that $TiSi_2$ is formed at the TiW/Si interface annealed at 660°C using rapid thermal process.[3]

The purpose of this study is to characterize the annealed TiW/Si interface. We discuss the electrical measurement results and the results of characterizing TiW/Si interface annealed in the range of 450 ~ 800°C in comparison with the W/Si interface.

2. Experimental

TiW films were deposited by rf sputtering from a $Ti_{0.3}W_{0.7}$ target onto n-type 10Ωcm <100> Si wafers. W films were also formed by sputtering. Prior to the metal deposition, native oxide on the Si wafers was removed by a HF solution. After deposition, the specimens were annealed at temperatures between 450 and 800°C in N_2 ambient for 30 minutes.

After removing TiW or W by a H_2O_2 solution, X-ray photoelectron spectroscopy (XPS), electron probe micro-analysis (EPMA) and X-ray diffraction (XRD) were used for analysis of the annealed TiW/Si and W/Si interface. Cross sectional transmission electron microscopy (TEM) was used to investigate the TiW/Si interfaces.

Patterned wafers were prepared for measuring contact resistance and junction leakage current. Cross-bridge Kelvin resistor of 0.6μm via diameter was used for measuring the contact resistance. Diode patterns with multiple contact holes were used for measuring the p/n junction leakage current.

3. Results and Discussion

Figure 1 shows the dependence of TiW/p+ and W/p+ contact resistances on the annealing temperature (measured with 0.6μm via diameter). In both cases, the contact resistance decreases with increasing annealing temperature. Annealing below 600°C, the contact resistance of TiW is higher than that of W. At 600°C, the contact resistance of TiW is almost equal to that of W. Above 600°C, the contact resistance of TiW becomes lower than that of W.

On the other hand, the contact resistance of TiW/n+ is always lower than that of W/n+ in this temperature range, *e. g.*, 45.2Ω for TiW and 56.0Ω for W annealing at 450°C, respectively. Therefore, when the annealing temperature is lower than 600°C, the difference of contact resistances is attributed to Schottky barrier heights with p-type silicon, 0.61eV for Ti and 0.45eV for W, respectively [4]. Above 600°C, the lowering of TiW/p+ contact resistance is attributed to silicidation.

The dependence of n/p junction leakage current on the annealing temperature is shown in Fig. 2. Considerably high leakage is occurred at 800°C for TiW/Si and at 700°C for W/Si, which is thought to be due to heavy silicidation.

To clarify the reaction mechanism, TiW/Si interface was analyzed with XPS and EPMA in comparison with W/Si interface after removing TiW or W by a H_2O_2 solution.

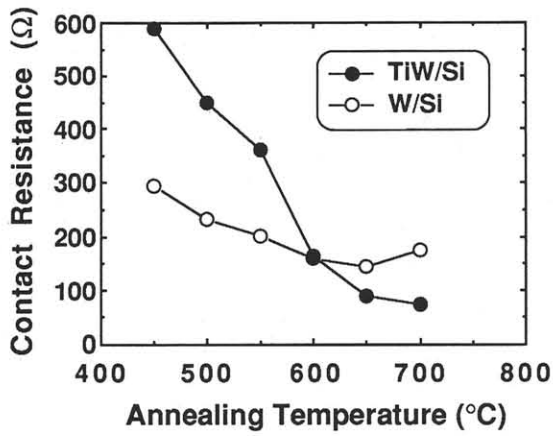

Fig. 1. The dependence of TiW/p+ contact resistance on annealing temperature, measured with 0.6μm via diameter.

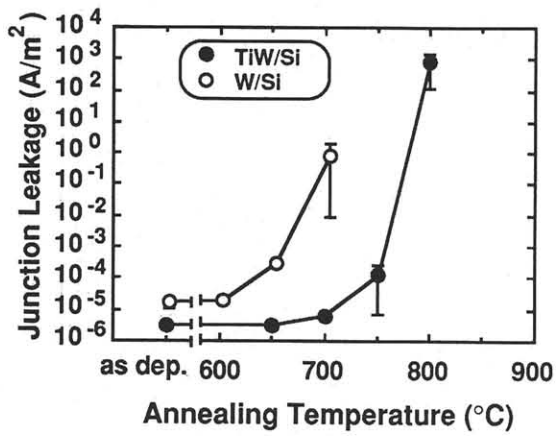

Fig. 2. Relation between n+/p junction leakage and annealing temperature.

Table 1. Chemical shift of Si(2p) XPS spectra, and atomic count of W and Ti based on fluorescent X-rays intensity with EPMA .

Sample	Annealing Temp. (°C)	XPS Chemical Shift Si(2p) (eV)	EPMA Atomic Count W (A.U.)	EPMA Atomic Count Ti (A.U.)
W/Si	500	4.42	-	
	550	4.37	< 1.0	
	600	4.39	< 1.0	
	650	4.15	22.2	
	700	4.15	57.0	
TiW/Si	500	4.39	-	-
	550	4.42	-	-
	600	4.24	1.5	< 1.0
	650	4.23	3.3	1.4
	700	4.25	5.1	2.3
	750	4.24	107.2	32.3

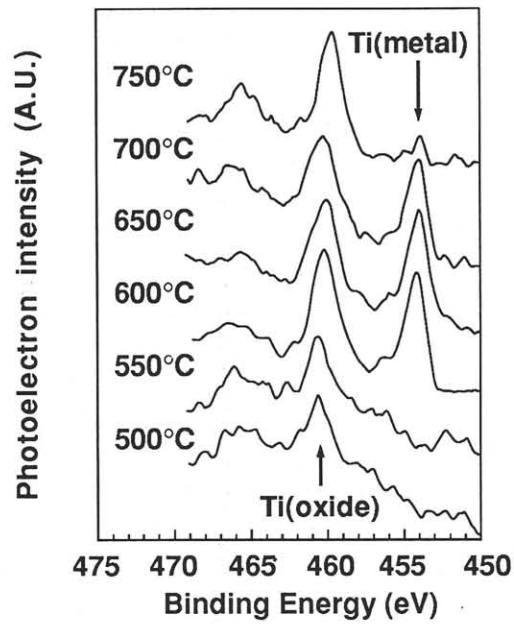

Fig. 3. XPS spectra of Ti(2p) from TiW/Si interface with various annealing temperatures. TiW is removed by H_2O_2 before XPS analysis.

The chemical shifts of Si (2p) spectra of XPS (the difference in peak positions of oxidized and unoxidized Si) and atomic count of residual Ti and W based on EPMA are listed in table 1. For W/Si, when the annealing temperature is 600°C or lower , the EPMA signal from W is lower than the detection limit. However, when the annealing temperature is 650°C or higher, the signal from W becomes strong. In addition, the chemical shift of Si(2p) decreases from 4.4eV to 4.15eV while the annealing temperature changes from 600 to 650°C. These results indicate that silicidation occurs at 650°C or higher. The decrease of the chemical shift is caused by silicide formation.[5] For TiW/Si, strong EPMA signals from Ti and W are observed at the annealing temperature of 750°C. However, in the range of 600 ~ 700°C, small amounts of Ti and W are detected. The decrease of the chemical shift of Si(2p) XPS spectra is observed while the annealing temperature changes from 550 to 600°C. XPS spectra of Ti(2p) from residual Ti with the annealed samples are shown in Fig. 3. The signal from metallic Ti in the range of 600 ~ 700°C is strong, however, it becomes weak at 750°C. From these results, we conclude that a silicide composed of Ti, W, and Si is formed even at 600°C, and the silicide formed in the range of 600 ~ 700°C is thin. While, above 750°C, the thick silicide is formed and the structure is thought to be changed compared to the lower annealing temperatures. In order to investigate the film structure, XRD analysis and TEM observation were done.

XRD spectra of the silicide at TiW/Si interface with various annealing temperatures are shown in Fig. 4.

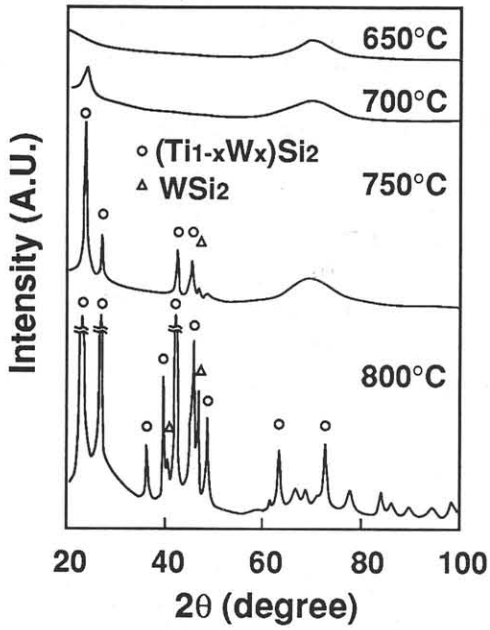

Fig. 4. XRD spectra of silicide layer at TiW/Si interface with various annealing temperatures. TiW is removed by H_2O_2 before XRD analysis, and Cu(kα) line is used.

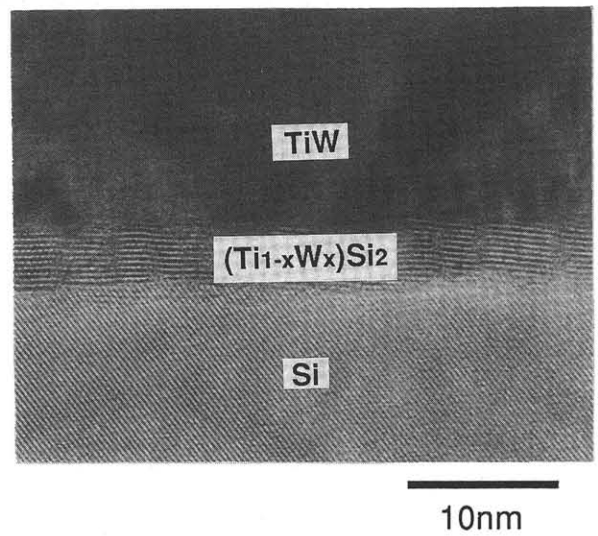

Fig. 5. A cross sectional TEM micrograph of TiW/Si interface annealed at 650°C.

When the annealing temperature is above 750°C, strong signals from $(Ti_{1-x}W_x)Si_2$ and WSi_2 are detected. Consequently, the thick silicide is a mixture of polycrystalline $(Ti_{1-x}W_x)Si_2$ and WSi_2. On the other hand, when the annealing temperature is 700°C, only a diffuse peak is observed at around $2\theta = 22°$. No peak of silicide is observed from the sample annealed at 650°C. This is because the amount of the thin silicide is very small as shown in table 1. A cross sectional TEM micrograph of TiW/Si interface annealed at 650°C reveals a thin layer of this silicide as shown in Fig. 5. A silicide layer is observed between TiW and Si substrate. The layer is epitaxial on Si, and the interplanar spacing of the layer agrees well with the (100) planes of $(Ti_{1-x}W_x)Si_2$ (0.399nm). [1, 6] The same layer was observed from the sample annealed at 600°C.

As shown in table 1, thick silicide of W/Si interface is formed at 650°C, and a similar result is reported for Ti/Si interface. [2, 5] However, in the case of TiW/Si interface, thick silicide is observed above 750°C. It is thought that the thin silicide layer, which is epitaxial on Si, has the ability to suppress heavy silicidation .

4. Conclusions

Annealed TiW/Si interfaces are characterized in comparison with W/Si interfaces. The TiW/Si interfaces are categorized by annealing temperatures into three groups.

(1) If the annealing temperature is below 600°C, silicidation is not observed, and the contact resistance with p-type silicon is higher than that of W, since Schottky barrier height of Ti is higher than W.

(2) Above 750°C, a heavy silicide, which is a mixture of polycrystalline $(Ti_{1-x}W_x)Si_2$ and WSi_2, is formed at the interface, and it breaks p/n junctions.

(3) In the range of 600 ~ 700°C, a thin silicide is formed at the interface. The layer is epitaxial on the silicon substrate and the phase is identified as $(Ti_{1-x}W_x)Si_2$. The epitaxial silicide layer lowers contact resistance and does not break p/n junctions, and suppresses heavy silicidation up to 750°C annealing temperature.

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