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Hot Carrier Effect of AC Stress on P-MOSFETs

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The hot carrier degradation under the AC stress was compared with that under the DC stress for the surface channel P-MOSFETs having 0.5μm gate length and 10nm gate oxide. The shift direction of drain current and threshold voltage becomes positive by the Drain Avalanche Hot Electron (DAHE) injection as the gate pulse voltage approaches the gate voltage with the maximum gate current and the shift direction gets negative by the Channel Hot Hole (CHH) injection as the gate pulse approaches the drain voltage. Moreover the shift direction depends not only on the pulse height but also on the rise/fall time as well as the frequency of the gate pulse as the peak voltage approaches the drain voltage since the ratio of the CHH injection time to the DAHE injection time is varied by these parameters.

1) Introduction

The device degradation due to hot carrier effect becomes increasingly important for the long-term reliability of VLSI in scaling down to the deep submicron range[1].

Hot carrier effect of AC stress has been studied to estimate the device life time of P-MOSFETs in the circuit operation. Many works have been so far performed for AC hot carrier degradation on N-MOSFETs to correlate with the degradation under DC stress. However little has been studied for hot carrier effects of AC stress on P-MOSFETs in spite of the importance in CMOS circuits. Therefore we have investigated the AC hot carrier effects on P-MOSFETs with half-micron gate length. In this paper, we will report on the new findings which are different not only from the AC hot carrier effects on N-MOSFETs[2] but also from the model previously reported on P-MOSFETs[3].

2) Device fabrication

The surface channel P-MOSFETs used in this study were fabricated with P^+ poly gate. The gate length is 0.5 μm, and the gate oxide thickness is 10 nm. Low energy B^+ implantation (10 keV) after pre-amorphization by silicon implantation was used to form the P^+ source/drain and the P^+ gate simultaneously after the side wall formation. The gate oxide was grown in HCl ambient at 810 °C. The side wall is silicon dioxide and its width is 120 nm.

3) Experimental

Fig.1 shows the measurement system for the AC hot carrier degradation. The AC stress was applied to the gate using the pulse generator. The applied voltage to the drain is kept constant. The source and the substrate voltages are set 0 V. For the AC stress condition, the frequency was varied from 100 Hz to 100 kHz with the rise and the fall time set equal and varied from 0.5 to 50 μsec. The pulse height was varied from 0 to -8 V. After the stress, the shift in threshold voltage (V_{TH}) and drain current (I_D) of P-MOSFETs were measured by the forward and the reverse mode.

To avoid the effect of the noise induced by the parasitic inductance of the measurement system[4][5], care was taken to reduce the noise during the AC hot carrier degradation. As a result, the maximum signal noise on the drain was suppressed to be less than 20 mV.

4) Results and Discussion

Fig.2 shows the gate and the substrate current characteristics of P-MOSFETs. The maximum gate current is at the gate voltage of -1.8 V when the drain voltage is -8 V. Fig.3 and Fig.4 present the comparisons of hot carrier degradation between the AC and the DC stress for I_D and V_{TH} shift, respectively, in the linear

region. The gate pulse height (V_P) and the DC gate voltage are changed from 0 to -8 V with the base line of the pulse (V_B) set equal to 0 V. The drain voltage (V_D) is -8 V. The effective stress time of the gate pulse was 500 sec, kept equal to the DC stress time by taking the duty ratio into consideration. It should be noted that the shift direction of I_D and V_{TH} in the small absolute values of the gate voltage is opposite to those in the large region. Moreover the differences in the shift between the AC and the DC stress increase as the gate voltage approaches the drain voltage. These results indicate that the Channel Hot Hole (CHH) plays a dominant role in the shift around the gate voltage equal to the drain voltage and the Drain Avalanche Hot Electron (DAHE) causes the major shift around the gate voltage of the maximum gate current. Namely when the gate pulse height is set equal to the drain voltage in the AC stress, CHH causes the negative shift in I_D and V_{TH} at the peak of the gate pulse, and DAHE causes the positive shift during the rise and the fall time of the pulse. This results in the increasing difference between the AC and the DC stress. Therefore the AC hot carrier degradation has to be estimated by taking CHH as well as DAHE into account and cannot be predicted simply by the gate current since no gate current is detected in the gate voltage range for the CHH injection. Interface states can be involved in the degradation for this gate voltage range.

Previous report[3] neglects the role of CHH in the AC hot carrier effect of P-MOSFETs, however, it is found that CHH plays an important part as mentioned above. To support this fact furthermore, we applied alternatively two DC stress (V_G=-1.8 V and -8 V) to the gate as given in Fig.5. It can be seen that CHH plays an important part in the hot carrier degradation of P-MOSFETs since the stress favoring CHH injection causes the large negative shift in V_{TH} and I_D.

Fig.6 gives the dependencies of the I_D shift on the rise/fall time and the frequency of the gate pulse of which height is -8 V equal to the drain voltage. It should be noted that the shift direction becomes negative as the rise/fall time and the frequency decrease due to the major role of CHH while the shift direction gets positive as the transitional time and the frequency increase due to the major role of DAHE.

Fig.7 gives the duty ratio dependence of the I_D shift as a function of the effective stress time under the AC stress with the gate pulse height of -1.8 V where the gate current is maximum and DAHE plays the major role. Under this stress the shift can be predicted from that under the DC stress by taking the duty ratio into account.

5) Conclusion

In this work the hot carrier degradation under the AC stress was compared with that under the DC stress for P-MOSFETs having 0.5 μm gate length and 10 nm gate oxide. The shift direction of I_D and V_{TH} becomes positive by the DAHE injection as the gate pulse voltage approaches the gate voltage with the maximum gate current and the shift direction gets negative by the CHH injection as the gate pulse approaches the drain voltage. Moreover the shift direction depends not only on the pulse height but also on the rise/fall time as well as the frequency of the gate pulse as the peak voltage approaches the drain voltage since the ratio of the CHH injection time to the DAHE injection time varies by these parameters. The degradation due to hot carrier is in proportion to the duty ratio of the gate pulse when the peak voltage is around the gate voltage for the peak gate current.

6)Acknowledgement

The authors would like to express their thanks to Drs. H. Komiya and T. Nakano for their continuous encouragement.

7) References

[1] M. C. Jeng et al., IEDM Tech. Dig., (1988) p386.

[2] M. M. Kuo et al., IEEE Electron Devices, ED-35 (1988) p1004.

[3] T. C. Ong et al., IEEE Electron Devices, ED-37 (1990) p1658.

[4] R. Bellens et al., IEEE Electron Devices, ED-37 (1990)p310.

[5] R. Izawa et al., IEDM Tech. Dig., (1990) p573.

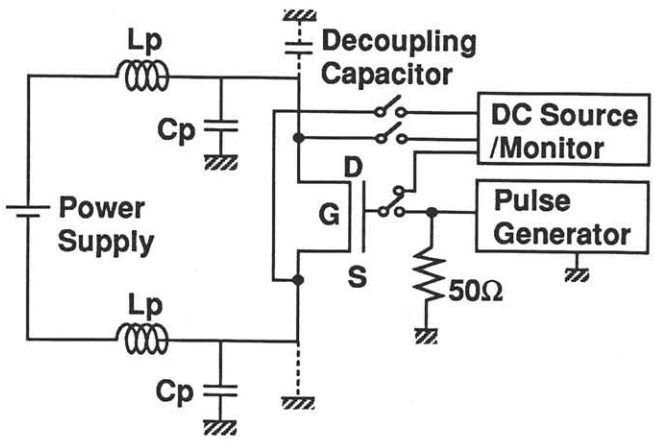

Fig.1 Measurement system for the AC hot carrier degradation

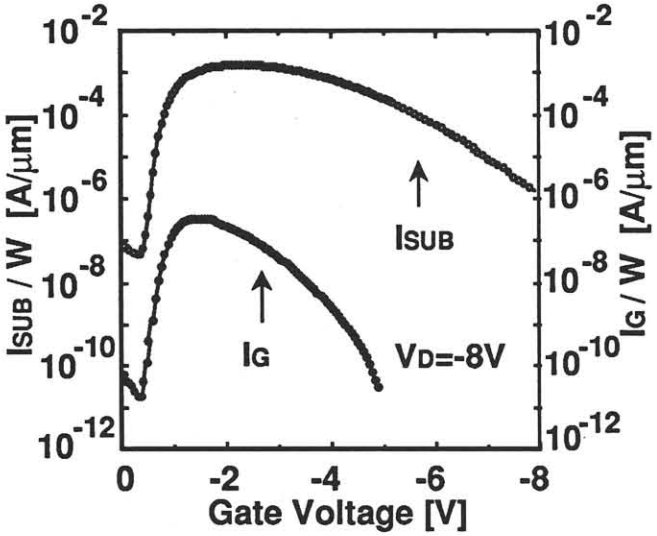

Fig.2 Substrate current(I_{SUB}) and gate current(I_G) with gate voltage.

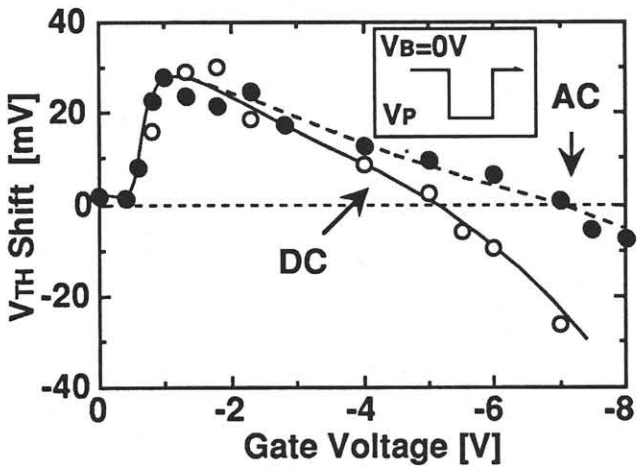

Fig.4 Threshold voltage shift of surface channel P-MOSFETs after AC stress and DC stress.
AC stress : V_D=-8V, duty ratio=50%, frequecy=10kHz, Δt=5μsec, stress time=1000sec
DC stress : V_D=-8V, stress time=500sec

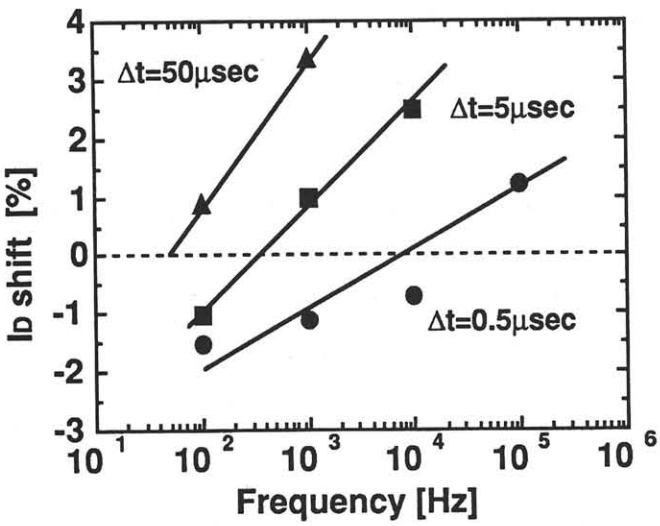

Fig.6 Frequency and transitional time dependencies of drain current shift under AC stress.
AC stress condition : V_D=-8V, V_P=-8V

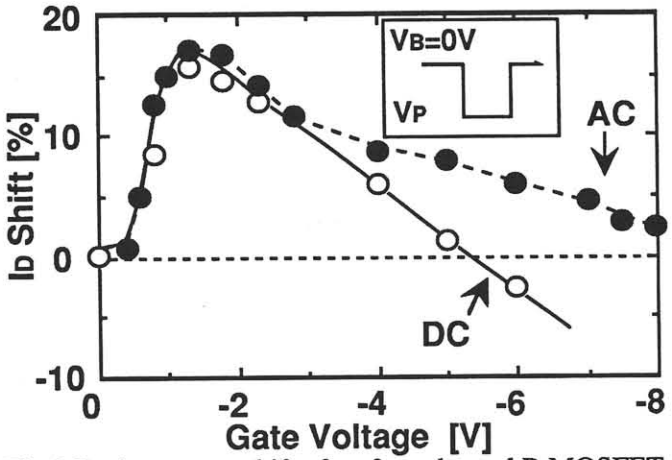

Fig.3 Drain current shift of surface channel P-MOSFETs after AC stress and DC stress.
AC stress : V_D=-8V, duty ratio=50%, frequency=10kHz, Δt=5μsec,stress time=1000sec
DC stress : V_D=-8V, stress time=500sec

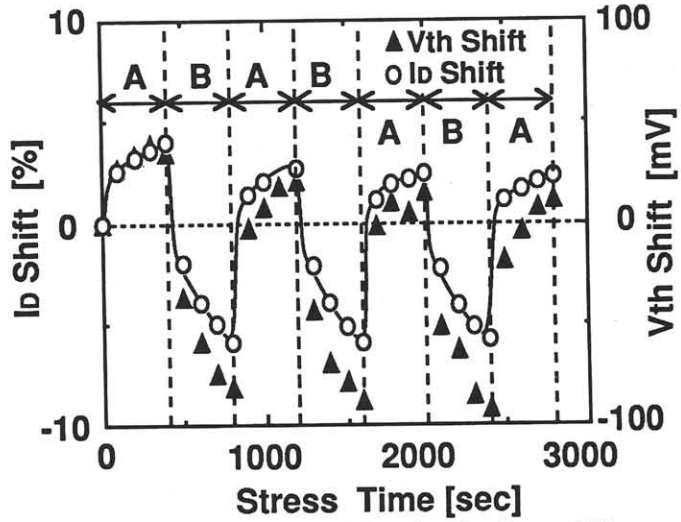

Fig.5 Drain current and threshold voltage shift in two DC stresses.
A : DAHE (V_D=-8V, V_G=-1.8V)
B : CHH (V_D=-8V, V_G=-8.0V)

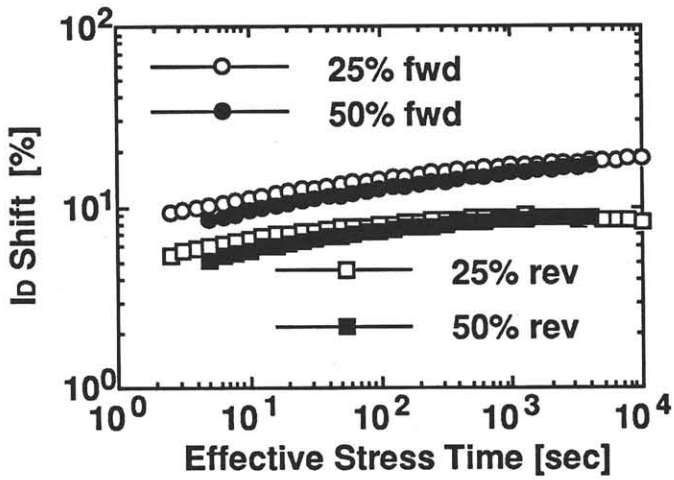

Fig.7 Duty ratio dependence of drain current shift in the forward(fwd) and in the reverse(rev) under AC stress.
AC stress condition : V_D=-8V,V_P=-1.8V