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Gate Oxide Deterioration Caused by Organic Contamination onto the Oxide

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The breakdown voltage of 10nm thick gate oxide was deteriorated showing increased B mode when photoresist was coated on the gate oxide and then stripped, though it was stripped using H_2SO_4/H_2O_2 supposed to be damage-free. The thicker the resist was, the lower the oxide yield was. No deterioration was observed when Al gate was used. An ashing added after the stripping recovered the breakdown characteristics in some degree. Total organic of the wet stripped wafer was 5 times as much as that of reference. We concluded that the organic contamination on the gate oxide was the cause.

INTRODUCTION

Many researchers have been studying on the integrity of gate oxide in ULSI. Many factors have been reported to be responsible for the degradation of gate oxide breakdown voltage: for example, Si material[1], metal contamination on Si [2], organic contamination on Si [3], and RCA cleaning on gate oxide[4]. Nothing, however, has been reported on the effect of organic contamination onto gate oxide. We reports in this paper that an organic contamination onto the oxide deteriorates its breakdown voltage.

Gate oxide would be coated with photoresist in the fabrication of SRAM which has buried contacts. In such a process, the photoresist directly formed on the oxide should be stripped off after etching of the oxide. Since it has been known that some kinds of ashing inflict metal contaminations[5] and/or charge-up damages[6] on oxides, a gate oxide deterioration may occur in that process. We had found that the breakdown voltage had actually been deteriorated due to the removal of the photoresist on the gate oxide.

A striking fact was that such a deterioration occured even when a wet stripping process with H_2SO_4/H_2O_2 was used to remove the photoresist. The purpose of this study is to clarify the mechanism of the deterioration.

We tested breakdown voltage with various stripping condition designed to identify the cause, and analysed organic materials on SiO_2 surfaces. Finally we concluded that organic materials remained on the gate oxide are responsible for the deterioration.

EXPERIMENTAL

MOS diodes were fabricated on 10Ω cm p-type (100) CZ-Si following the process shown in Fig.1. Active areas were defined using a LOCOS process, and 10nm thick gate oxides were grown in dry O_2 added with HCl at 1050℃. Photoresist of 2μm in thickness with a novolak resin base was then coated, and stripped by ashing and/or wet stripping treatments. Wafers for reference samples were treated with wet stripping without photoresist coating, and wafers for control received no treatment in this step. After an acid pre-cleaning, a 400nm polysilicon was deposited,

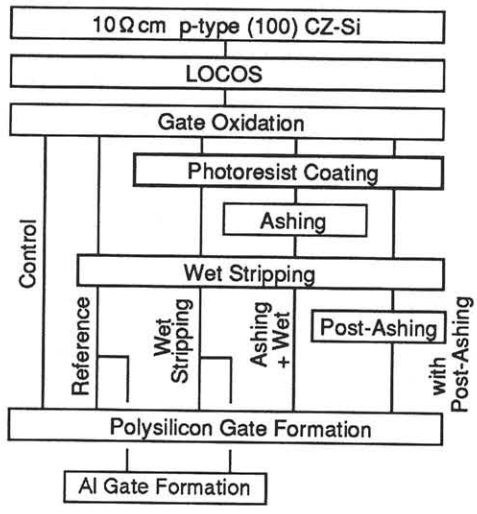

Fig.1 Flow chart of the process used for the sample fabrications in this study. Condition names used in this paper are written vertically.

followed by phosphorus doping at 900℃ and lithographic definition of gates. On some wafers, instead of polysilicon, 1μm thick Al gate electrodes were formed, in which process the highest temperature after the gate oxidation was 450℃.

A single wafer plasma asher was used for the ashing treatment. Wafers were treated in 3 different plasma modes: O_2 RIE(Reactive Ion Etching), O_2/CHF_3 DF(Down Flow, nominal as revealed), and O_2 DF. Sulfuric acid added with hydrogen peroxide was used for the wet stripping treatment at 130℃, followed by deionized water rinse. A barrel type plasma asher was used for an ashing treatment after the wet stripping ("Post-Ashing") putting dummy wafers both in front of and behind the sample wafers to avoid the charge-up[6].

The breakdown characteristics were measured with a ramp voltage method, and the yield mentioned below was defined as the percentage of MOS diodes which were not broken below 4.3mA/cm² gate current. Organic materials on the wafer surfaces were analyzed using PYRAN SYSTEM (RUSKA LABORATORIES, INC.), which is equipped with two thermal desorption systems and a gas chromatography system.

RESULTS AND DISCUSSION

The diodes fabricated with the photoresist process on their gate oxides showed lower yield due to increased B mode than that of the control samples, though they were treated with the wet stripping supposed to be " damage-free". On the other hand, when the gate oxides were 20nm thick, both diodes with the photoresist process and control samples exhibited almost the same breakdown yields. Hence, this phenomenon will become serious problem for the near-future SRAM, which is to have the thinner gate oxides.

Fig.2 shows the yields of MOS diodes having

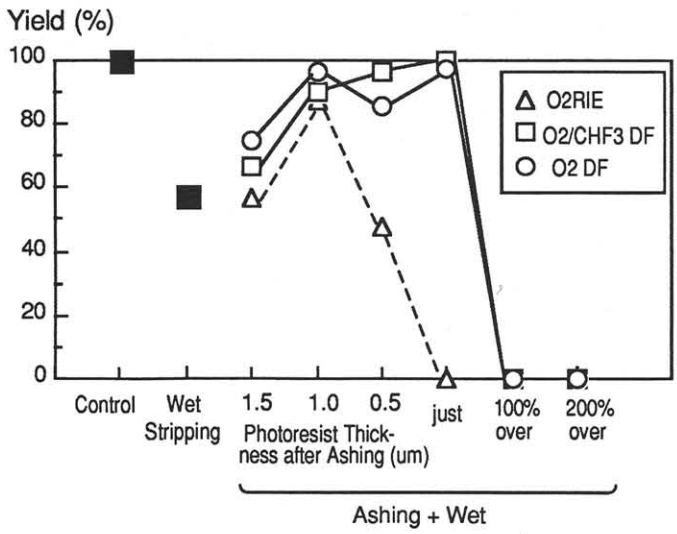

Fig.2 Dependence of the MOS diode yield on the ashing condition and on the combination of ashing and wet stripping.

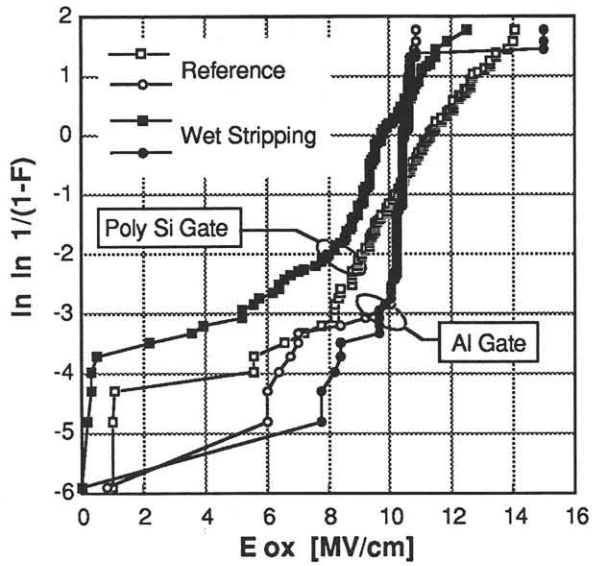

Fig.3 Breakdown field distributions of poly-Si gate and Al gate MOS diodes. Eox is oxide field at which each diode broke, F is cumulative failure.

150μm square areas fabricated with various ashing/stripping conditions. In the over ashing region (two rightmost of Fig.2), the yields are very low as we expected.

Metal contaminations from the photoresist[5] is one possible cause since the penetration of some metal elements into gate oxide reduces its breakdown voltage * . A charge-up damage is another possible cause, though the breakdown of MOS capacitors have been reported only for plasma processing after the gate electrode definition[6, 7]. In any case, these ashing processes should be categorized into damaging process [8].

By the way, the defect density of gate oxides varied from one experimental lot to the other: the wafers lead results shown in Fig.2 exhibited much more defect densities than that of Fig.3 and Fig.4. The dependences discussed below, however, were confirmed for several lots of wafers; they stood when the defects were detectable by the breakdown voltage evaluation.

The problem of the main subject exists in the wet only and under ashing region (the center of Fig.2). In this region, the yield becomes lower as the photoresist to be wet stripped becomes thicker, except for O_2 RIE, which could inflict a damage before reaching to just ashing.

This dependence suggests that the deterioration originates in residual materials, which were neither detected with optical microscope nor with SEM. The materials should remain because of a removal ability insufficiency of the wet stripping treatment.

*T.Nakanishi: Ext. Abstr. 38th Spring Meeting Jpn. Soc. Appl. Phys. and Related Soc.(1991) 28a-V-7.

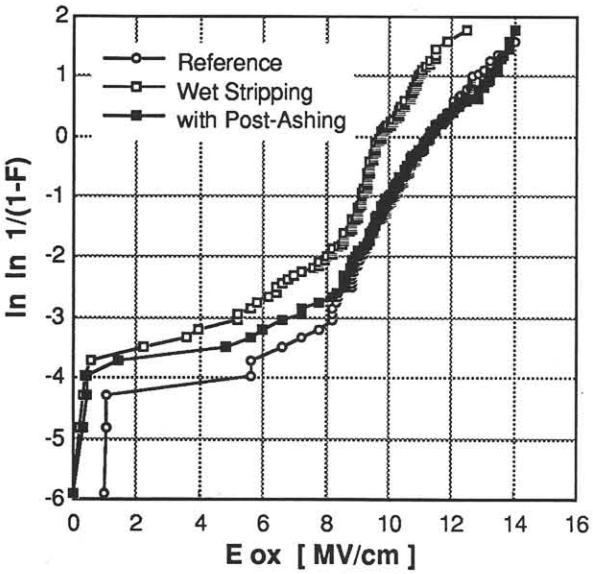

Fig.4 Breakdown field distributions of poly-Si gate MOS diodes. Eox is oxide field at which each diode broke, F is cumulative failure.

Metal contamination can hardly explain this dependence. Because the metal contained in the resist would be condenced by ashing into the remaining portion of the resist, the thinner resist remaining after ashing could give the same metal contamination.

Electrostatic discharge might be responsible, because some wet treatments cause charging-up and photoresist might make a difference between wafers in the charging-up. To reject this rare possibility, we tested breakdown voltages with low temperature process.

Fig.3 shows the breakdown voltage distributions of the polySi gate and the Al gate MOS diodes, with 6.9cm² oxide area each. The Al gate diodes were not deteriorated by the wet stripping of photoresist while the polySi gate diodes were. In other words, the actual deterioration did not occur during the photoresist stripping, but occured during the polySi gate formation. Consequently, ESD cannot be the cause.

To confirm more the working hypothesis of the residual material mentioned above, we examined the effect of the post strip ashing.

Fig.4 shows the results. The ashing treatment added after the photoresist stripping ("with Post-Ashing") recovered the breakdown characteristics in some degree. This means that the residual material responsible for the deterioration can be decreased with the ashing, and hence metal contamination cannot be the cause of the deterioration.

Consequently, the gate oxide deterioration should be caused by the residual organic material from the photoresist on the oxide. In fact, as shown in Table 1, total organic were much more detected from the wet stripped wafers than others.

Table 1 Total organic on gate oxide analysed with PYRAN SYSTEM

Preparing condition	Total organic (g/cm^2)
Reference	3.6×10^{-9}
Wet Stripping	1.7×10^{-8}
Ashing + Wet	2.0×10^{-9}

Many sources of organic contaminations on Si surface has been reported[9] ; and hence, we will point out that organic contamination onto gate oxide should be eliminated carefully.

CONCLUSION

The thin gate oxide was deteriorated with the photoresist process. We found that organic impurities would remain on the gate oxide after the wet stripping of the photoresist coated on the oxide, and concluded that the organic contamination was the cause of the deterioration; other possible causes were rejected with several experiments. We will point out that general organic contamination onto thin gate oxide can deteriorate the oxide.

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