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Scaling and Physical Limitations of Quantum Flux Parametron (QFP) Devices

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This paper reports the scaling principle and physical limitations of QFP devices. Three dimensional scaling and constant thickness scaling reduce device delay by the scaling factor of k., while heat dissipation does not limit the scaling of QFP. London's penetration depth, thermal noise and quantum limitation should be seriously taken into consideration to determine the minimum device size. QFPLSI's fabricated by a 0.35 μm technology would realize 10^7 gate QFP supercomputer on 1 cm^2 chip, operating at more than 100 GHz. In addition, QFP circuits, fabricated by high Tc superconductor technology will properly operate at 77 K by choosing appropriate power dissipation of QFP circuit.

1. INTRODUCTION

The progress of silicon LSI technology has made it possible to realize supercomputers with more than Giga FLOPS performances. It is necessary to shrink the processor size down to 1 cm cubic for further decrease of machine cycle time within the next ten to twenty years for Tera FLOPS supercomputing, when circuit delay and power dissipation should be reduced by several orders of magnitude. Quantum Flux Parametron (QFP) device [1,2] is one of the most promising candidates for the high performance supercomputer. The quite notable advantage of QFP devices is the extremely low power consumption and fast switching speed, as compared in the speed-power diagram in Fig. 1 [2]. A supercomputer, utilizing 10^7 gate QFP devices dissipates only 10 mW (1nW/gatex10^7), while conventional silicon LSI system should melt down due to the high power density of about 10 kW (1mW/gatex10^7). This paper describes the scaling principle and physical limitations of QFP devices to evaluate the possibility of realizing a supercomputer on 1 cm^2 chip. It also evaluates the possibility of fabricating QFP circuits based on the high Tc superconductor material technologies.

2. SCALING PRINCIPLE OF QFP DEVICES

2.1. Operation Principle

QFP device operates preserving flux quantum in the superconductor loop, and the optimum circuit parameter is expressed by the following equation [2].

$$8\, I_j \cdot L = \Phi_0 \qquad (1),$$

where, I_j, L and Φ_0 denotes critical current of Josephson Junction, load inductance and flux quantum, respectively. Equation (1) is always applied in scaling the QFP devices in the following discussions.

Switching speed and power consumption of QFP device are expressed by the following equation,

$$\tau = \sqrt{LC} \qquad (2).$$

$$P = (\Phi_0/\tau)^2 / R \qquad (3),$$

where, C and R are capacitance and resistance of QFP, respectively. Power dissipation of the present 5μm QFP device is around 10^{-9} W/gate, and the switching delay is around 15 ps, with 25μA critical current [1,3].

2.2 Scaling principle

Three scaling principles of QFP devices, three dimensional, constant thickness and power increase-decrease, are discussed in this section. The former scales down the lateral dimensions as well as thicknesses of the

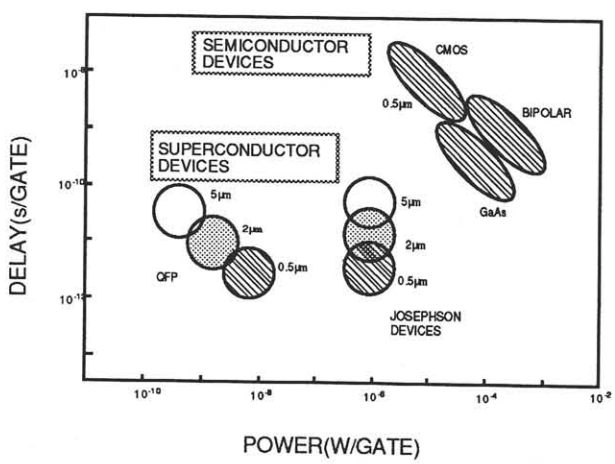

Figure 1 Comparison of switching speed and power consumption of semiconductor devices and superconductor devices

superconductor and insulator layers by a factor of k. The middle shrinks only the lateral dimensions, and was taken into consideration in case such physical limitations as London's penetration depth and mean free path of the superconductor limits the scaling. The last one was taken into consideration to eliminate the quantum and thermal limitations. The scaling factor, k, dependence of speed and power consumption are summarized in Table 1.

Table 1 Scaling of QFP by three principles

	L	C	R	I_J	τ	P
3-Dimension	1/k	1/k	1	k	1/k	k^2
Const. thick.	1	$1/k^2$	k	1	1 / k	k
Power I/D	1/k	1	$\sqrt{k}$	k	$1/\sqrt{k}$	$1/\sqrt{k^3}$

3. PHYSICAL LIMITATIONS OF QFP DEVICES

3.1. Cooling limitation

The maximum heat dissipation from solid surface is in the order of 0.7 W/cm^2 in liquid helium [4], and $7x10^8$ gates/cm^2 can be integrated on one QFPLSI chip. Assuming that one QFP device area requires about 20 times of the minimum dimension area (pixel) and one QFP gate consists of 5 QFP devices, the minimum dimension is 1/10 of the minimum gate pitch.

$1/\sqrt{7x10^8x10^2} \approx 1/(2.5 \times 10^5) = 0.04\ \mu m$ (4).

Thus the minimum dimension of a device is around 0.04 μm, and $7x10^{10}$ devices can be integrated on 1 cm^2 chip when the heat dissipation of QFP is 10^{-9} W/gate. The same derivation was conducted for cooling system of 10 W/cm^2 (liquid nitrogen) and 100 W/cm^2 (fluoro carbon). Figure 2 summarizes the relationship between heat dissipation of one gate and the minimum dimension of the device, as well as the maximum number of devices integrated on a 1 cm^2 chip. The figure indicates that a 10^7 gate supercomputer can be integrated on a 1 cm^2 chip by helium cooling if the heat dissipation is lower than 7×10^{-8} W/gate and minimum dimension of 0.35 μm can be employed. In the case of liquid nitrogen cooling, the heat dissipation can reach as high as 7×10^{-7} W/gate.

3.2. London penetration depth

QFP operation requires the preservation of flux quantum in superconductor loop. London penetration depth (λ_L)[4] determines minimum achievable dimension of QFP's. Three dimensional penetration of the magnetic field into the superconductor material limits the thickness and width of a superconductor line to be more than $2\lambda_L$. Typical λ_L of the materials spread out between 30 and 300 nm [4,5]. Nb has the shortest value of λ_L=31.5 nm, and the smallest dimension that QFP device can reach by the current technology and material is around 0.1 μm. Materials with smaller penetration depth are necessary to fabricate smaller QFPLSI's.

3.3. Thermal noise and quantum limitations

QFP devices misoperate if thermal noise energy and quantum energy exceeds the device energy, which is

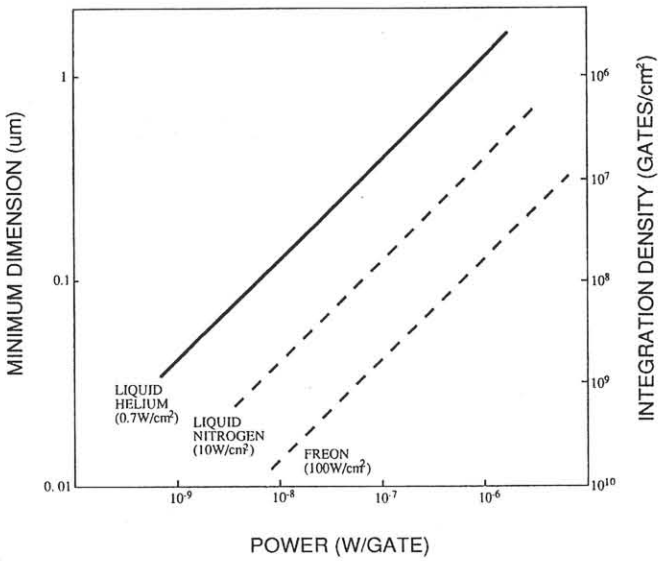

Figure 2 Relationship between power dissipation of gate, minimum dimension and maximum number of devices on a 1 cm^2 chip

expressed by the following equation [2],

$E_Q=(\Phi_0/\pi)I_J$ (5).

The switching number is 10^{27}, assuming that a 10^8 QFP device operates at 100 GHz, 4 phase, for one year without misoperation. Therefore, the error rate should be less than 10^{-27}. The quantum limitation should also be taken into consideration, in which the product of switching time and energy stored in the superconductor loop should exceed the macroscopic tunneling energy, which will be explained in the later section.

4. MANUFACTURING LIMITATIONS

The scaling limitations are also assessed from the manufacturing technology point of view. The variations of structural parameters, such as barrier oxide thickness, pattern size and surface morphology should be taken into considerations. However, the present technologies [6] already indicate that the only processing parameter which should be precisely controlled is the pattern size, which will be discussed in the later section.

5. DISCUSSIONS

5.1. Comparison of power dissipation

In the case of semiconductor devices, the limitation is determined by the heat dissipation by fluorocarbon cooling system, measuring around 100 W/cm^2. Even if the most efficient cooling scheme [8] is employed, the integration density would not exceed 10^6 gates/cm^2. Therefore, the minimum dimension in such LSI is,

$1/\sqrt{100x10^6} = 1 \times 10^{-4} = 1.0\ \mu m$ (6)

The number represents the average integration density, and does not necessarily mean that minimum dimension of silicon LSI's cannot reach sub-half micron. Almost the same discussion could be applied for the LSI's employing conventional Josephson Junction devices, in

which the cooling is limited by the heat removal of 0.7 W/cm^2 by liquid helium. The maximum integration level is around 10^6 gates/cm^2, and the minimum feature size is also limited to around 1.0 μm.

5.2. Speed power diagram of QFP device

The speed-power diagram of QFP gate is depicted in Fig. 3. The broken lines show the thermal and quantum limitations of 10^{-100} error rate, which should be enough to guarantee the error free operation of future supercomputers. The results clearly depict that the present devices should reliably operate at 4 K. They also indicate that reliable QFP operation with the present critical current will be limited by the quantum limitation if the minimum dimension reaches around 0.25 μm, which is overcome if the current density is increased by a factor of 3. They clearly show that quite reliable operation of 10^7 gate QFP supercomputer on 1 cm^2 chip is ascertained by employing QFP devices fabricated by a 0.35 μm technology and dissipation energy of 2 x 10^{-8} W/gate.

5.3. Manufacturing technology innovation

Control of critical current, I_J requires control of both critical current density J_J and junction area, A. Variation of I_J on pattern size is reported, as shown in Table 2 [6]. The following discussion assumes that these variations are due to the variations of junction area ΔA and tunnel oxide thickness Δs, that the pattern size variation Δl is constant and is independent of the pattern size l, and that the tunnel current density variation, ΔJ_J, is constant for all dimensions. The results indicate that variation of the Josephson Junction critical current is mainly dominated by the pattern size variation of around 0.03 μm. Therefore, advanced lithography technology should make it possible to realize well controlled Josephson Junction characteristics.

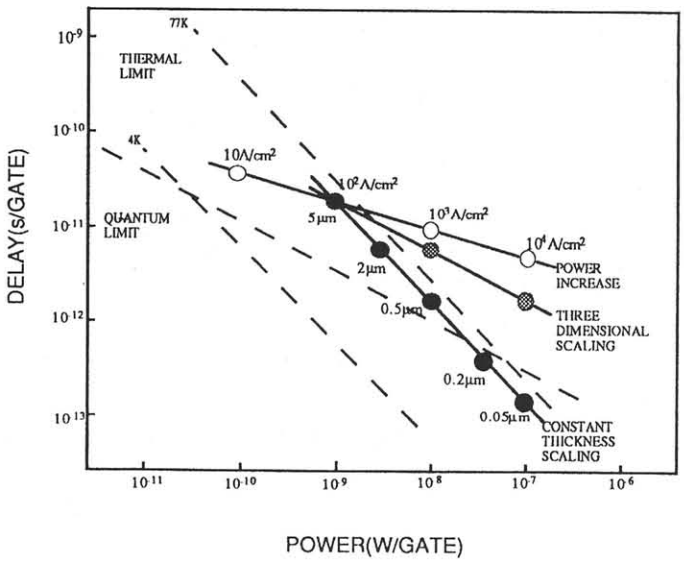

Figure 3 Speed power diagram of QFP device scaling principle, with quantum, thermal and other physical limitations.

Table 2 Analysis of the critical current variation

minimum pattern size (mm)	variation of critical current (%)	variation of patternsize (mm)
10.0	0.5	0.025
2.0	2.0	0.02
1.0	7.0	0.035

5.4. QFP devices by high Tc Josephson Junctions

High Tc application of QFP circuit is discussed here. As described previously, QFP devices can operate with non-hysteretic Josephson Junctions, which could be the only junction characteristics that current high Tc technology can realize [7]. The minimum necessary energy for the reliable QFP device operation at 77 K is indicated by a broken line in Fig. 2. The results depict that constant thickness scaling of the QFP devices down to 0.25 μm is well within the thermal and quantum limitations if the critical current is increased by a factor of 3, and London penetration depth is cleared. Heat dissipation of up to 1 x 10^{-6} W/gate at an integration density of 10^7 gates/cm^2 can be cooled at 77 K in liquid nitrogen as indicated in Fig. 3. These results clearly show that a supercomputer on 1 cm^2 chip is achievable based on high Tc technologies.

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