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Structural and Electrical Improvement of GaAs on Si by Multi-Step Rapid Thermal Annealing Treatment

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One multi-step rapid thermal annealing (MSRTA) technique is proposed and optimized to improve structural and electrical properties of GaAs epi-layer MBE grown on Si substrate. MSRTA is superiod to conventional single step RTA in improving structural properties and in restraining deep level EL2 formation. Meanwhile,MSRTA can provide higher electron mobility and implantor activation in Si-implanted GaAs/Si. Better parameters uniformity of GaAs/Si MESFETs has been obtained, too.

Introduction:

Due to the large lattice and thermal mismatch between GaAs and Si, much structural and electrical imperfection is found in GaAs MBE grown on Si substrate than in bulk GaAs. RTA (rapid thermal annealing) is an effective technique to improve epi-GaAs crystalline quality on Si as to increase PL (photoluminescence) intensity and decrease RBS (Rutherford backscattering/channel mode) yield [1],and as to reduce threading dislocation density and eliminating twin and stacking faults[2]. However, after conventional single step RTA (SSRTA), slip line and crack may appear in GaAs epi-layer, especially when GaAs epi-layer thickness excesses 4 μm. Simultaneously, high density of EL2 is introduced in MBE grown GaAs on Si after SSRTA[3], the reason is not well understood.

In this paper, the experimental results utilizing multi-step rapid thermal annealing (MSRTA) to improve GaAs/Si structural and electrical properties are summarized. MSRTA may avoid creating slip line and crack in GaAs epi-layer. After MSRTA, evident improvements have been obtained on both crystalline quality as shown by PL, TEM and RBS. The density of deep level EL2 in MBE GaAs/Si samples introduced by MSRTA can be significantly lower than that by SSRTA. Compared with SSRTA, MSRTA can provide higher electron mobility and implantor activation in Si-implanted GaAs/Si wafers. Better parameters uniformity of GaAs/Si device has been obtained, too.

Experiments and results:

GaAs layers were grown on vicinal Si (100) substrates by MBE. InGaAs/GaAs strained layer superlattice and thermally straind layers were grown before the growth of semi-insulated GaAs in order to filter threading dislocation. MESFETs active regions were separated by mesa etching, Ni/AuGe/Ni/Au was used for Ohmic metallization and Ti/TiW/Au for Schottky metallization.

RTA was conducted using a Heatpulse 410 system. For SSRTA, the GaAs/Si wafers were heated to 900°C for 10 seconds. For MSRTA, a typical temperature profile is shown in Fig.1, where two additional temperature steps are introduced as intermediate steps at which MBE GaAs/Si wafer is supposed to have minimum thermal mismatch stress. In Fig.1, the parameters tr1, tr2, tf1, tf2 are set to be zero and t1=t2=t3=10 sec. in general. So, GaAs epi-layer on Si will not be enforced to deform from tensile to compressed in a very short time in MSRTA. In this case, GaAs/Si wafer deformation and stress inside GaAs epi-layer can be greatly released. It is not only effective to eliminate slip line and crack formation, but also helpful to restrict dislocation immigration and define structural defects within strained layers region and near GaAs/Si interface, as shown by TEM cross-section picture.

PL intensity was measured on as-grown GaAs/Si samples and samples after SSRTA, MSRTA treatment, the results are shown in Fig.2. Take peak A as example, MSRTA achieves eightfold increase of PL intensity with respect to non-RTA and some 10% increase with respect to SSRTA.

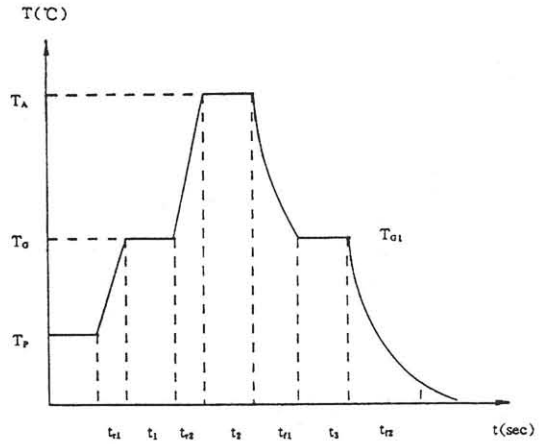

Fig.1 Temperature profile of MSRTA

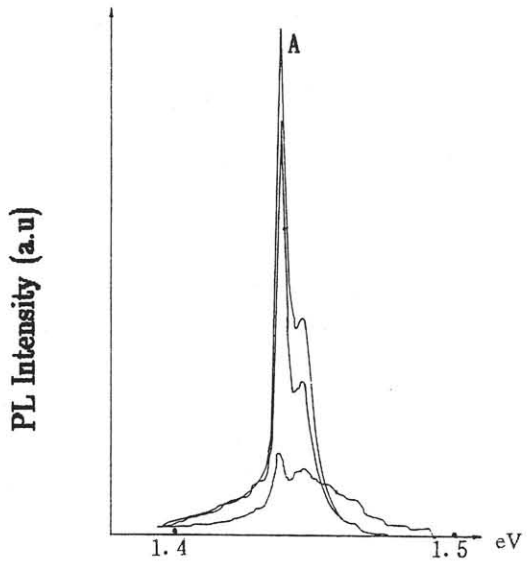

Fig.2 PL intensity measurements on as-grown (lower), SSRTA (middle) and MSRTA (upper) GaAs/Si wafers

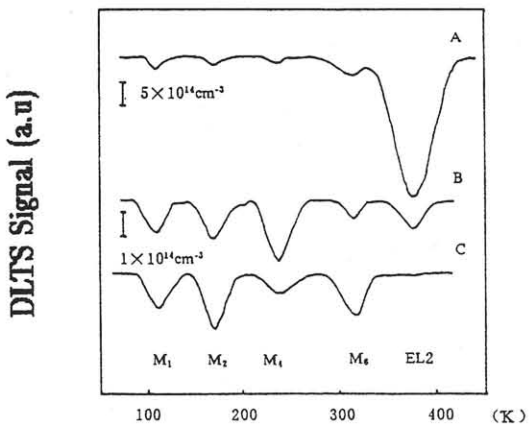

Fig.3 DLTS measurement on SSRTA and MSRTA processed GaAs/Si samples
A: SSRTA, 900°C, 10 s
B: MSRTA, t1=t2=10 s, t3=20 s
C: MSRTA, t1=t2=10 s, t3=2 s

It is noticed that, the concentration of deep level EL2 in a MSRTA processed GaAs/Si sample can be significantly lower than that in a SSRTA processed saple, as detected by DLTS and shown in Fig.3.

Compared with SSRTA, MSRTA can provide higher electron mobility and implantation activation in Si-implanted GaAs/Si wafers. Better parameters uniformity of GaAs/Si devices have been obtained, too. These results are quite similar to bulk GaAs case as reported in reference [4] and [5].

Discussion:

In thermoelasticity, the stress in GaAs/Si wafer during rapid thermal process due to the thermal mismatch between GaAs and Si can be greatly released in MSRTA than in SSRTA. That is why MSRTA can eliminate slip line and crack formation and restrain dislocation immigration. The facts that dislocation is gettered and confined within strained layers region and near GaAs/Si interface, structural defects or damage can be restored at 600 C add more possibility for MSRTA to improve structural perfection and obtain higher activation of implantor. MSRTA produces less EL2 in MBE GaAs is probably an indicaton that EL2 formation in MBE GaAs/Si after RTA is related to samples deformation and stress magnitude inside GaAs epi-layer.

Reference:

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