Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials, Yokohama, 1991, pp. 553-555

Estimation Method for Charge Build-Up on Gate Oxide during Bias ECR Plasma Deposition

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A simple method for estimating charge build-up on gate oxide during plasma processing has been proposed. The method is based on the observation that metal oxidation at the SiO_2-metal interface is accelerated by an electric field, which is formed by electrons diffused from the SiO_2 surface to the metal surface. The electron-induced charge build-up can be estimated by measuring the thickness of metal oxide by ellipsometry analysis. Applying the method to bias ECR plasma deposition, it is confirmed that metal oxidation thickness is strongly associated with the degradation in gate oxide yield.

I. Introduction

The thickness of gate oxide in MOS devices has become thinner with higher packaging density in VLSI. Thus, gate oxide breakdown due to the charge build-up during plasma processing has become a more serious problem. The mechanism of the charge build-up has usually been examined by measuring the electrical characteristics of MOS or MNOS devices[1),2)]. The estimation method by using such devices takes it long time to obtain experimental results.

A simple method for estimating charge build-up is proposed, which determines the charge build-up without the fabrication of MOS devices. The method is based on the observation that metal oxidation is accelerated by an electric field set up by electrons even under a low temperature[3)]. When a two-layer film consisting of SiO_2 on a metal is exposed to plasma, metal oxidation occurs at the SiO_2-metal interface due to the electric field set up by electrons diffused from the SiO_2 surface to the metal surface. Consequently, the charge build-up during plasma processing can be estimated by measuring the metal oxide thickness using ellipsometry analysis.

This paper describes experiments carried out using molybdenum(Mo) as a metal. Applying this method to bias Electron Cyclotron Resonance plasma deposition[4)] (bias ECR), Mo oxidation at the SiO_2-Mo interface was measured, and the relationship between Mo oxidation thickness and gate oxide yield of MOS diodes was studied.

II. Mo Oxidation at the SiO_2-Mo Interface

Mo was used because of its smooth surface morphology suitable for ellipsometry analysis. After Mo was deposited on an insulator by sputtering, SiO_2 was deposited by bias ECR as shown in Figs. 1(a), (b). Next, the oxide at the SiO_2-Mo interface as shown in Fig. 1(c) was analyzed using ellipsometry. Figure 2 shows the dependencies of Mo oxide thickness measured by ellipsometry on SiO_2 deposition time. The SiH_4/O_2 mixed gas pressure and microwave power of ECR plasma deposition are 1.0 mTorr and 600 w, respectively, and rf power density is $1.17 W/cm^2$. For ECR plasma deposition without rf bias, Mo oxide thickness is almost constant below 50A, where the natural Mo oxide thickness is below 20A. For bias ECR with rf bias, Mo oxide thickness increases rapidly when deposition time exceeds 200 sec. Figure 3 shows the AES depth profiles with and without rf bias for a deposition time of 350 sec. For a long sputtering time from 10 min to 25 min, both Mo and oxygen signals in depth profiles with rf bias co-exist, while those without rf bias disappear within a short period. This result suggests the presence of Mo oxide for rf bias and also shows the validity of ellipsometry analysis.

Figure 4 shows the substrate temperature dependence of Mo oxide thickness. The Mo oxide thickness of samples for CVD-SiO_2 deposited at 350-450°C on ECR-SiO_2 at RT was also measured by ellipsometry. A comparison of Mo oxide thickness for rf bias shown in Fig.2 with that for CVD-SiO_2 on ECR-SiO_2 shown in Fig.4 reveals that, in spite of a higher deposition temperature, the Mo oxide thickness for CVD is extremely less than that for ECR plasma deposition with rf bias. This result confirms that Mo oxidation is mainly accelerated by rf bias but not by substrate temperature, i.e., oxidation is caused by an electric field set up by rf bias during bias ECR plasma deposition.

III. Charge Build-Up Phenomenon

The gate oxide yield was investigated using an MOS diode with a gate oxide thickness of 110A. The SiO_2 was directly deposited on the poly-Si gate MOS diodes. The gas pressure and microwave power of ECR plasma deposition are 1.0 mTorr and 600 w, respectively. Figure 5 shows the dependencies of yield on deposition time. For ECR plasma deposition without rf bias for the antenna ratio(electrode/gate area, $10^6 um^2/10^4 um^2$) 100, the yield is a constant 100%. This means that ECR plasma without rf bias does not influence the charge build-up. For bias ECR with rf bias, the yield decreases with an increase in deposition time and also in antenna ratio. Particularly, above an antenna ratio of 25, the yield is decreased drastically. Thus, gate oxide yield degradation is attributed to the charge build-up due to rf bias. Figure 6 shows the flat band voltage V_{fb} characteristics of MOS diodes. Compared with V_{fb} of a reference sample, V_{fb} shifts with rf bias, which means that V_{fb} shifts with the electron trapping.

A comparison of the plots for rf bias shown in Fig.2 with those in Fig.5 reveals that deposition time dependencies of Mo oxide thickness are consistent with those of the yield as shown in Fig.7. The yield decreases sharply with increasing Mo oxide thickness. Therefore, the yield can be estimated by measuring the Mo oxide thickness without fabricating MOS devices.

IV. Summary

An estimation method for the charge build-up has been proposed. Applying this method to bias ECR plasma deposition, the following results were obtained; (i) Mo oxidation at the SiO_2-Mo interface is caused by rf bias during bias ECR plasma deposition. (ii) The gate oxide yield with bias ECR plasma deposition is degraded by charge build-up in the plasma. (iii) The gate oxide yield degrades with increase in Mo oxide thickness.

Therefore, charge build-up can be estimated by measuring Mo oxide thickness.

Acknowledgments

The authors would like to thank Dr. Eisuke Arai, Dr. Hideo Oikawa, Mr. Hideo Yoshino, Mr. Hideo Akiya, and Mr. Seitaro Matsuo for their advice and encouragement. They also extend thanks to Mr. Hiroshi Ishibashi for his assistance in the experiments.

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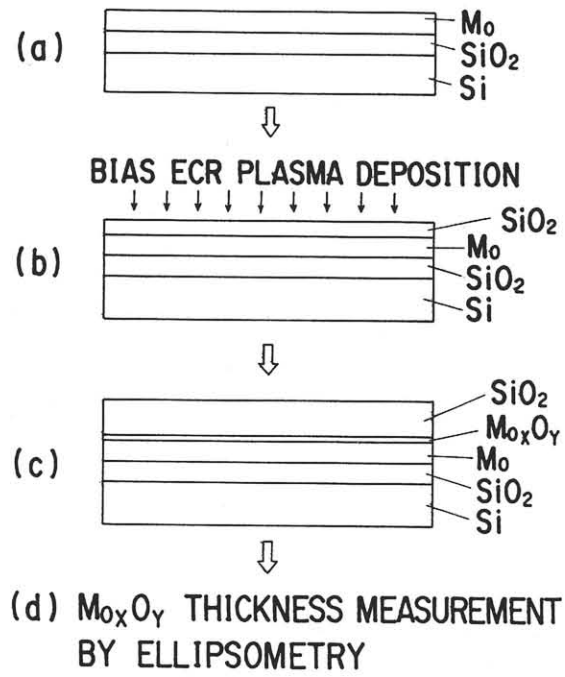

Fig.1 Key features of charge build-up estimating method.

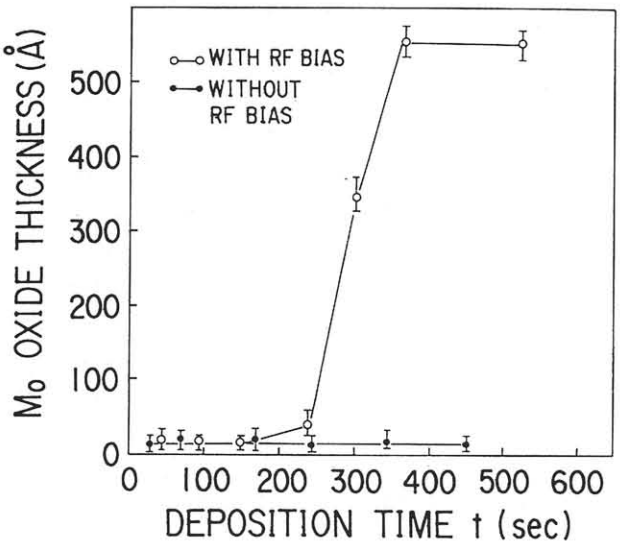

Fig. 2 Dependence of Mo oxide thickness on deposition time. Microwave power is 600 w. Gas pressure is 1.0 mTorr. Rf power density is 1.17 W/cm^2.

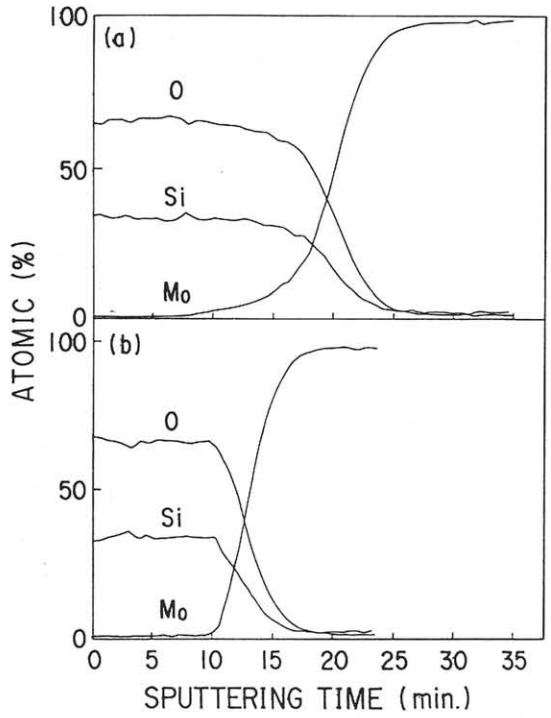

Fig. 3 AES depth profiles. (a) with rf bias (b) without rf bias

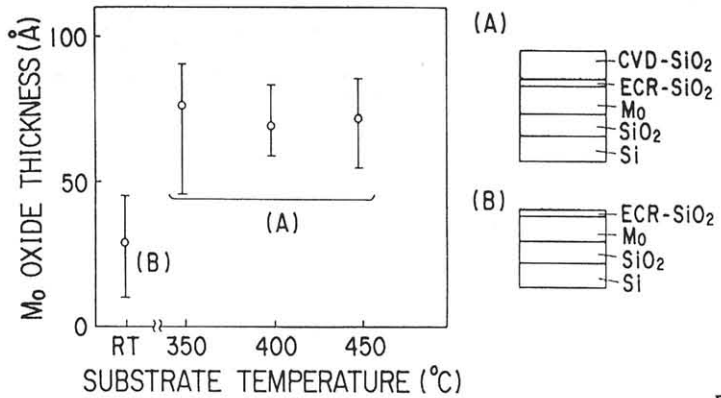

Fig. 4 Relationship between Mo oxide thickness and substrate temperature.

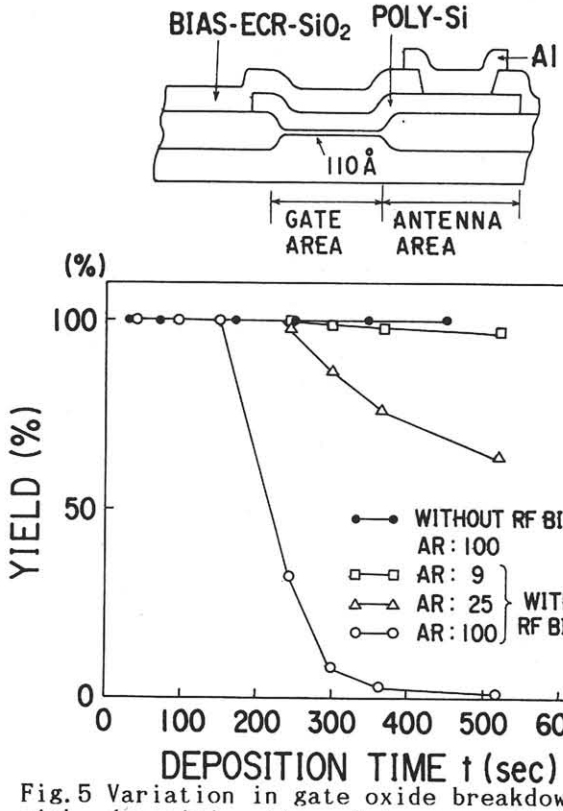

Fig. 5 Variation in gate oxide breakdown yield with deposition time. Antenna ratio (AR) is electrode area/gate area. Gate area is 10000 μm^2 constant.

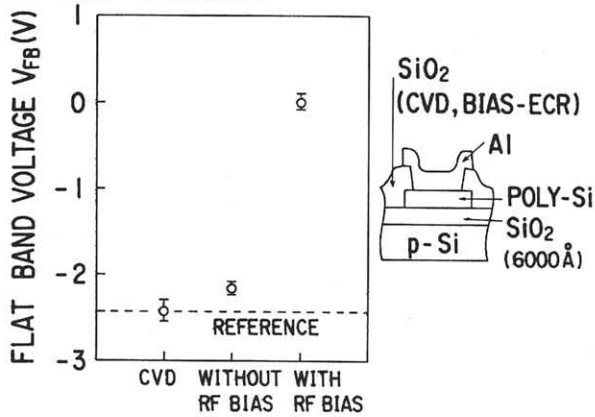

Fig. 6 Flat band voltage V_{fb} characteristics.

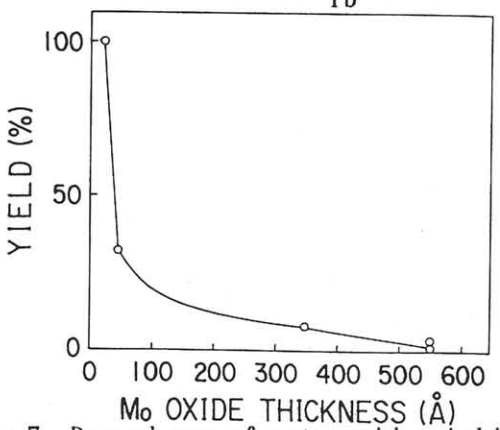

Fig. 7 Dependence of gate oxide yield on Mo oxide thickness.