Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials, Yokohama, 1991, pp. 559-561

The Optimization of In-Situ Thermal Cleaning Focused on Surface Microroughness for Future Si Epitaxial Growth

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A few nanometer surface microroughening caused by high temperature in-situ thermal cleaning (pre-baking) before CVD Si epitaxial growth process is studied using STM. Among three pre-baking condition, i.e. H_2-100Torr, Ar-100Torr and High vacuum, Hydrogen ambient pre-baking shows the minimum degree of microrougheing. The native oxide formed in H_2SO_4:H_2O_2=4:1 cleaning prior to wafer loading is effective in preventing the surface microroughness.

1. Introduction

As the device pursues finer geometry and advanced performance, the Si epitaxial layer becomes more important to be employed as the highly integrated CMOS in which the short channel effect and the carrier mobility are critical. Every application employs the structure that the thin epitaxial layer with low concentration is formed on the substrate with high concentration.

Meanwhile in the case of forming extremely thin epitaxial layer of 500nm or less, the microroughness of the epi-substrate interface and that of the epitaxial layer surface needs to be carefully watched. Figure 1 shows the experimental results when the surface microroughness was measured with the computerized surface profiler. In this experiment, the wafer was first immersed in to 5% NH_4OH solution at the room temperature to intentionally make it surface rough. Then the epitaxial layer of 1.8um was formed on this wafer surface by means of the CVD method. The surface microroughness before the epitaxial growth is well reflected on the after epitaxial growth. This surface microroughness on the epitaxial layer can not be improved even by following thermal oxidizing and by removing it. It is clear that, in order to secure the surface flatness after the epitaxial growth, the wafer surface must be controlled to be sufficiently flat until the very moment that the epitaxial layer formed. It has been reported that the microroughness of several nanometers on the wafer affects the breakdown of thin gate oxide of MOS[1].

Taking these problems into account, authors have conducted experiments to examine the thin epitaxial layer growth with the CVD method. The growth process is divided into two stages : the in-situ cleaning (pre-baking) process and the epitaxial growth process. This article describes the surface microroughening caused by pre-baking process. And it refers to the influence of trace impurities on microroughness and to the effect of the native oxide formed intentionally on wafer surface to protect microroughness.

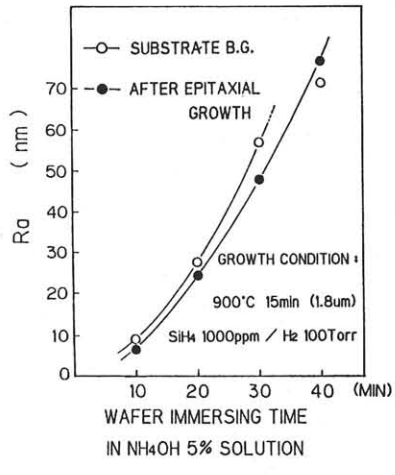

Fig.1 The influence of substrate surface roughness on Epitaxial grown surface.

2.Experimental method

The unit used in the experiment is the high vacuum compatible horizontal reactor in which the temperature is raised with the RF dielectric heating. The susceptor employs the SiC-coated graphite. The ultimate pressure of this unit is $3x10^{-9}$Torr level can be maintained. As for the source gas to form the epitaxial layer, SiH_4, which is diluted to 1000ppm with H_2, is introduced. The gas distribution system employs the ultra clean gas delivery system. The maximum trace impurity in the gas used is H_2O, and its concentration is several parts per billion or less at the point of use. The surface microroughness of the wafer is examined with the wide coverage type STM (Scanning Tunneling Microscope). We use the "Ra", means the average roughness, value to explain the roughness. The other expression "Rmax", means the peak to vary of the roughness, can estimate 10 times "Ra".

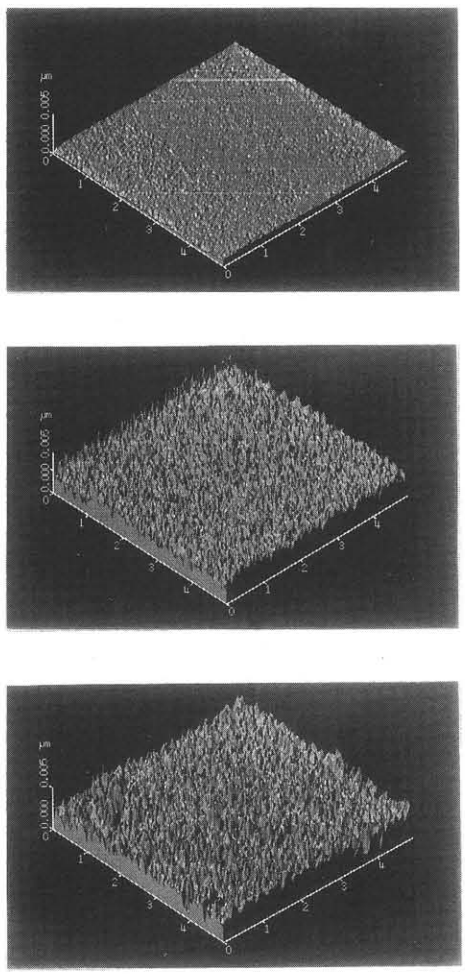

Fig.2 The STM images of wafers surface pre-baked as follows;
(a) H_2-100Torr, 940C, 15min.
(b) Ar-100Torr, 940C, 15min.
(c) High Vacuum, 940C, 15min.

The P-doped n(100)CZ wafer with the resistivity of 8-12 cm is used in the experiment.

3.Result and discussion

The H_2 (100Torr) ambience and the vacuum ambience (10^{-7}Torr order during pre-baking) were employed this time. In addition, the Ar (100Torr) ambience was also studied.

Figure 2 shows the STM images of wafers processed as follows : the native oxide on the wafers was removed first with 0.5% DHF and then the wafers were pre-baked under the conditions of (a)-(c) respectively. As shown in Figure 2, it is learned the wafer surface gets deteriorated in the other ambience than the H_2 ambience.

Figure 3 show the degree of the surface microroughness without epitaxial growth when the temperature and the time are changed in the H_2 (100Torr) ambient and Ar (100Torr) ambient pre-bake applying the parameter of Ra, respectively.

It has been reported that the bare Si surface is etched when it reacts with oxygen atoms existing in the ambience in trace volume and SiO is produced[2)3)4)].

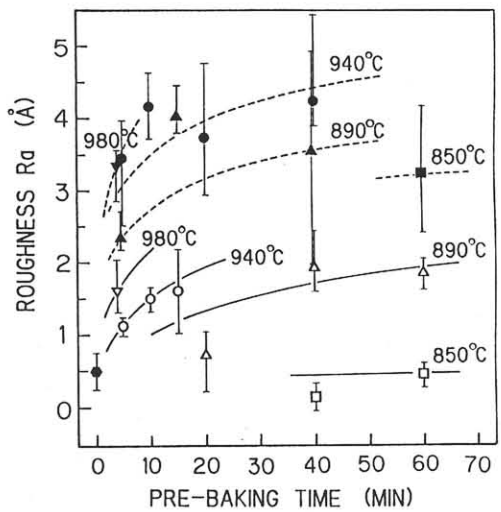

Fig.3 The degree of surface microroughness Ra when the temperature/time are changed in H_2 and Ar pre-bake.
The dashed line shows Ar-100Torr baking
The solid line shows H_2-100Torr baking

Figure 4 shows the degree of the surface microroughness when the partial pressure of O_2 + H_2O are changed under high vacuum pre-baking.

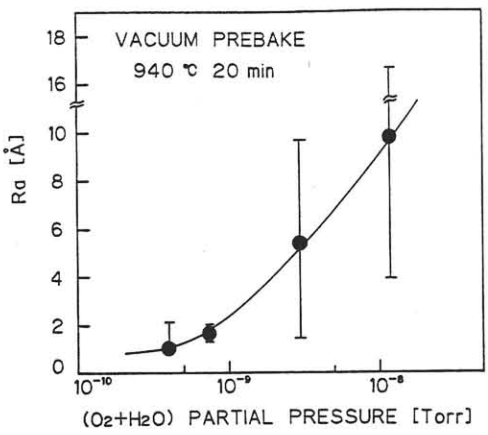

Fig.4 The influence of O_2+H_2O partial pressure on surface micro-roughness under high vacuum ambient pre-bake.

From these results, the degree of surface microroughness strongly depend on the existence of trace impurities (H_2O, O_2 molecules). The allowable impurity partial pressure, without surface roughening, should be less than 10^{-9}Torr under high vacuum or in inert gas ambient pre-baking.

The previous experimental results indicate that it is not favorable to expose the bare Si surface to the pre-bake process. Based on the findings, the experiments were conducted to examine the effect of the native oxide as the protective film for the Si surface. In this experiment, the native oxide with the thickness of 0.7nm was formed on the wafer surface in the H_2SO_4:H_2O_2 cleaning (H_2SO_4:H_2O_2 = 4:1). This oxide (hereunder referred to as "HS oxide"), features the lowest desorption temperature among the oxides grown in various kinds of acid cleaning[5]. And we confirm that this HS oxide film can be removed by both of H_2 (100Torr) and high vacuum ambient pre-baking with 940C, 15min. This means the wafer surface is protected for 15min.

The vacuum ambient pre-bake and the H_2 ambient pre-bake are compared in terms of the surface microroughness, shown in figure 5. In the case of H_2 ambient pre-bake, Ra values are distributed around 1.2A, showing the minimum roughening. These Ra values are close to reference value obtained from the non-processed wafer. We also confirmed the MOS diode breakdown statics of wafers pre-baked under H_2 ambient. The samples which applied HS oxide have higher breakdown voltage than the samples without it. On the other hand, the Ra values vary in the wide range in the case of the vacuum ambient pre-bake. This indicates the desorption of HS oxide at high temperature does not take place in a uniform manner over the entire wafer surface in the vacuum ambience.

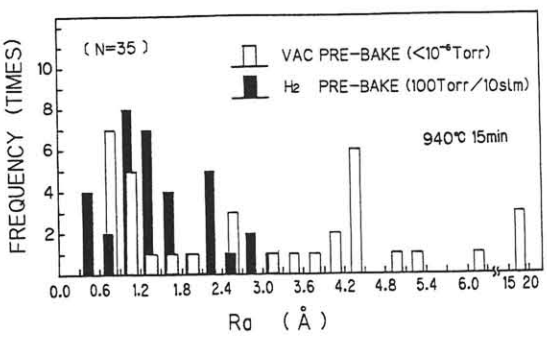

Fig.5 The deviation of surface micro-roughness compared with H_2 and High vacuum ambient pre-baking. Wafers are prepared with HS oxide before baking.

4.Conclusions

The effect of the pre-bake process on the wafer surface was studied in various ambiences in terms of the microroughness. The H_2 ambient pre-bake has been found very effective against the surface microroughness. It has been also learned the native oxide formed in the H_2SO_4 + H_2O_2 cleaning is effective in suppressing the surface microroughness. This native oxide can be removed in the 15 min pre-bake at 940C in the H_2 ambience.

5.Acknowledgment

The series of this studies were conducted at Super Cleanroom at Electric Communication Laboratory of Tohoku University.

Reference

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