Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials, Yokohama, 1991, pp. 725-726

$In_{0.5}Ga_{0.5}As$/InAlAs MODFETs on GaAs Substrates Grown by Low Temperature MBE

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We have proposed InGaAs/InAlAs MODFETs on GaAs substrates using InGaAs or InGaAlAs graded buffer layer (GBL) , and reported the importance of using wide gap material for the GBL to reduce the undesirable residual carrier accumulation at the interface between the GBL and the layers on top of it for the improvement of MODFET characteristics[1]. This paper describes a drastic reduction of the residual carrier and the improved MODFET characteristics by using an wide-gap InAlAs GBL and the low temperature MBE growth.

A schematic cross-sectional view of the $In_{0.5}Ga_{0.5}As$/InAlAs MODFET structure used in this work is shown in Fig. 1. It was grown on a (100)-oriented S.I. GaAs substrate by MBE and consists of an undoped GaAs layer grown at 580 °C, an InAlAs GBL grown at 350 °C, an InAlAs barrier layer and an active InGaAs/InAlAs MODFET structure. The layers on top of the GBL were grown either at 350 °C (**LT MODFET**) or 500 °C (**HT MODFET**). The compositions of In and Al in the GBL were changed linearly from AlAs to $In_{0.49}Al_{0.51}As$. The doping level of Si in the N-InAlAs was $5x10^{18}/cm^3$.

Figures 2 and 3 show the carrier profiles in the HT and LT MODFET structures obtained by C-V measurements, respectively. In Fig.2, the carrier accumulation with peak concentration of about $1x10^{17}/cm^3$ was observed near the interface between the InAlAs GBL and undoped InAlAs barrier layer. On the other hand, no accumulation of the residual carriers was observed for the LT MODFET structure. The electron mobility at room temperature of 11,100 $cm^2/Vsec$ for the LT MODFET structure was obtained with an electron concentration of $3x10^{12}/cm^2$. This mobility was higher than that of 7500 $cm^2/Vsec$ for the HT MODFET structure. The origin of the residual carrier was not clear from the SIMS analysis, but is considered to be related to some kind of defects created by the temperature raise or the growth interruption after growing the GBL[1].

Figures 4 and 5 show the characteristics of preliminary HT and LT MODFET, respectively. The gate width and the gate length were 150 μm and 1μm, respectively. The LT MODFET clearly show low output conductance and good pinch-off characteristics as compared with those of the HT MODFET. Moreover, the kink in the I-V characteristics was not observed in the LT MODFET , which is probably due to the well-known effect of the low temperature buffer layer as reported for the lattice-matched InGaAs/InAlAs MODFETs[2]. The higher transconductance of 270mS/mm was also obtained for the LT MODFETs.

In conclusion, we have shown that high-mobility InGaAs/InAlAs MODFET structures with reduced residual carrier concentration can be realised

on GaAs by the use of wide-gap InAlAs graded buffer layer and low temperature MBE growth.

Reference

1) K.Inoue, J.C.Harmand and T.Matsuno, Journal of Crystal Growth **111** (1991) pp.313-317
2) A. S. Brown, C. S. Chou, M. J. Delaney, C. E. Hooper, J. F. Jensen, L. E. Larson, U. K. Mishra, L. D. Nguyen and M. S. Thompson, 1989 IEEE GaAs IC Symposium, pp.143-146

n-$In_{0.5}Ga_{0.5}As$	100Å
undoped $In_{0.49}Al_{0.51}As$	200Å
n-$In_{0.49}Al_{0.51}As$	100Å
undoped $In_{0.49}Al_{0.51}As$	30Å
undoped $In_{0.5}Ga_{0.5}As$	300Å
undoped $In_{0.49}Al_{0.51}As$	2000Å
InAlAs graded buffer layer ($AlAs \rightarrow In_{0.49}Al_{0.51}As$)	9750Å
undoped GaAs	2000Å
S.I. GaAs Substrate	

Fig.1 Schematic cross-sectional view of the $In_{0.5}Ga_{0.5}As$/InAlAs MODFET structure with InAlAs graded buffer layer grown on S.I.GaAs substrate.

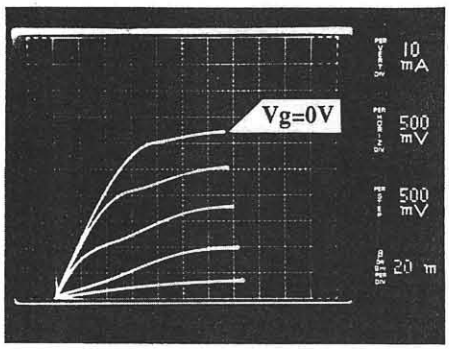

Fig.4 FET characteristics of **HT MODFET.**

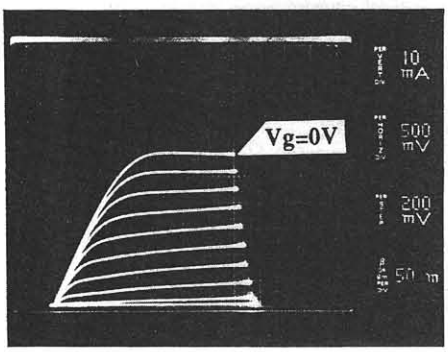

Fig.5 FET characteristics of **LT MODFET.**

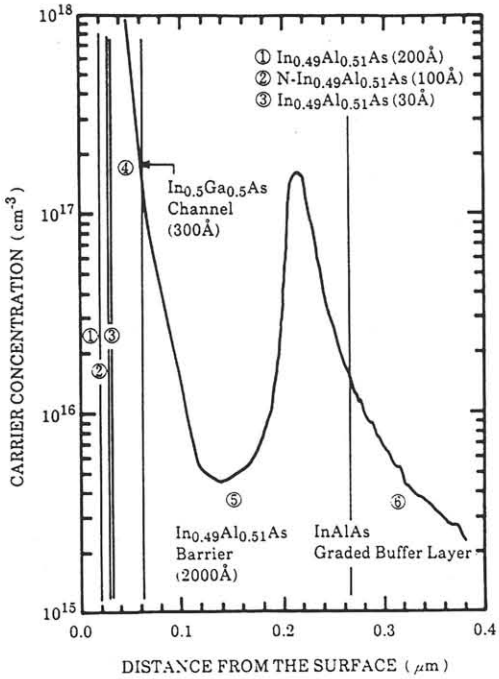

Fig.2 Carrier profile in the **HT MODFET** structure obtained by C-V measurement.

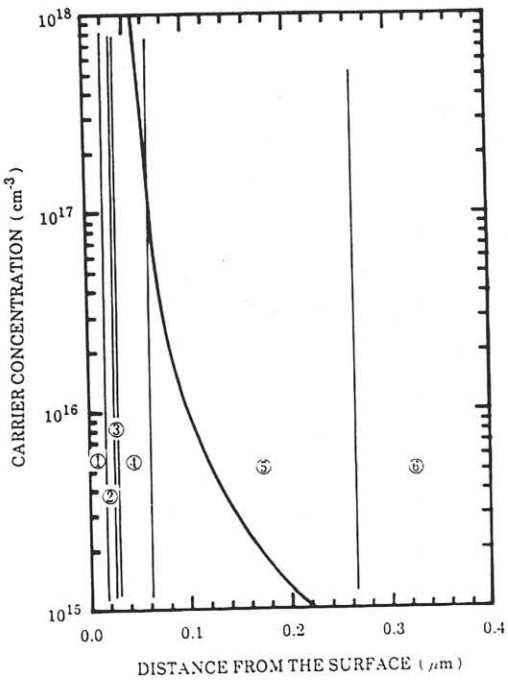

Fig.3 Carrier profile in the **LT MODFET** structure obtained by C-V measurement.