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Integration of a PIN and Vertical JFET for Photodetector OEIC

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The integration of a PIN and a VJFET is useful for OEIC since the structure is compact and has potentially very high power and speed capabilities. The fabricated PIN has low leakage current, below 50nA at 10V bias. But VJFET shows low transconductance and does not show full drain current cut off. Thus, a modified VJFET is also fabricated which incorporated W for the gate resistance reduction. The W deposited on p-layer improves the VJFET characteristics significantly. Also a simple model for VJFET is proposed including the space charge limited curent effects.

I. Introduction

Optoelectronic integrated circuits(OEIC's) have been studied by many researchers for their benefits, such as increased performance, reduced cost, size and weight reductions, and less stringent power requirements. This situation is very similar to the case where the development of integrated electronic circuits have given benefits to the conventional electronic circuits .

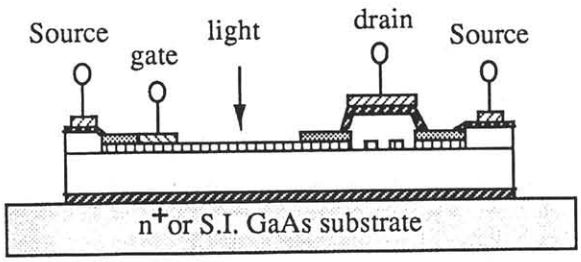
The horizontal type OEIC's using MESFETs, back-to-back Schottky diodes, laser diodes(LD's), etc., are easy to fabricate in the sense that fine line lithography technology and the other well-developed technologies can be directly applied but the usual LD threshold current in these cases requires relatively large transistor area. But the vertical type OEIC's using vertical transistors solve the problems mentioned above. Vertical transistors such as heterojunction bipolar transistor, vertical FET, etc., inherently have high power and speed capabilities. Thus, if the parasitic capacitances, gate or base resistances can be reduced by design improvement, good OEIC would be obtained.

Also the vertical cavity surface emitting LD's with high reflectance stacked mirrors[1] or conventional horizontal LD's match well with the vertical transistor in integration. But, usually the photodetector does not match well with the light emitting devices.

Recently, the vertical integration of a light source and a vertical transistor has been made and the electronic devices match well with the optical devices[2]. But, the photo-detection part of the vertical type OEIC's has not been developed so far. In this paper, a vertical junction FET(VJFET) and a modified VJFET, of which the gate area is a PIN diode are to be presented. In this modified VJFET, W layer is inserted to reduce the gate parasitic resistances.

II. Structure and Fabrication

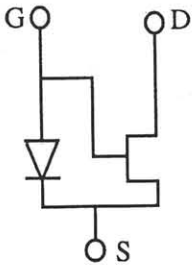
Figure 1 shows the schematic diagram of the fabricated photodetector OEIC. The structure is originally that of the vertical FET whose gate is changed from tungsten to p-GaAs to enhance the junction characteristics for lower dark current in photodetector. Epitaxial growth is done by atmospheric-pressure MOCVD. The layers are consist of n^+-GaAs buffer(about 1 to 2 μm), n^--GaAs(about 1 to 2 μm) and 0.2μm intrinsic carbon doped p-GaAs. We used either n^+ or S.I. GaAs substrates. The 200~300nm SiO_2 is deposited by RF sputtering and then SiO_2 pattern etching and VJFET area grating etching by wet etchant are followed. The grating has a period of 10μm and line/space is about 5μm/5μm. The 2nd epitaxial growth is done considering the fact that the effective growth rate over the grating area is 4 times greater in this experiment than that over the far GaAs region away from the drain region. It is increased because sources for growing migrate on the SiO_2 region to reach the GaAs seed if the migration length is smaller than about 100μm. If the migration length is greater than 100μm, homogenous reaction occurs and droplets of (Ga)(As) form. These droplets are porous poly GaAs formed on SiO_2 region. And then the poly GaAs was etched away by wet etchant. The AuGe/Ni/Au for n-ohmic metal and Au/AuZn/Au for p-ohmic metal are used. Annealing is done at 370°C for 1min 30sec. The individual device characteristics are shown in figure 2. The dark current of PIN diode is about 50nA at 10V bias. The VJFET has a low transconductance and does not show full cut-off



$\square n^-$-GaAs ▨ n metal ▨ p metal ▩ SiO_2

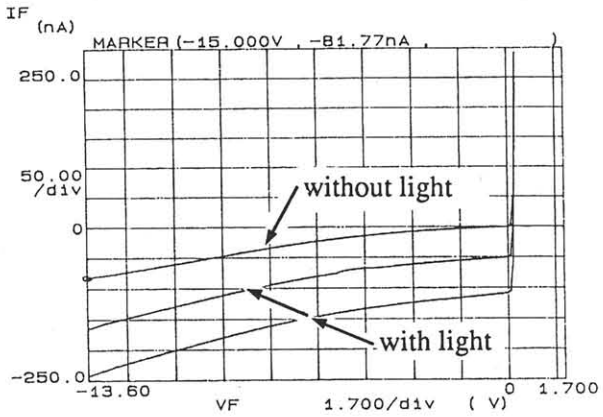
▨ p GaAs ▨ n^+-GaAs

(a)PIN-VJFET Schematic

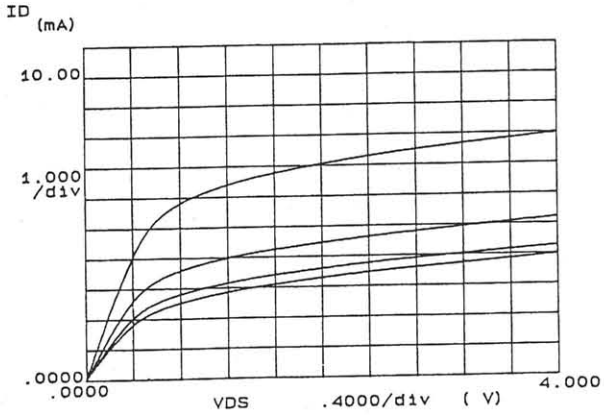


(b)Circuit Diagram

Figure.1 PIN-VJFET Structure



(a) PIN light response



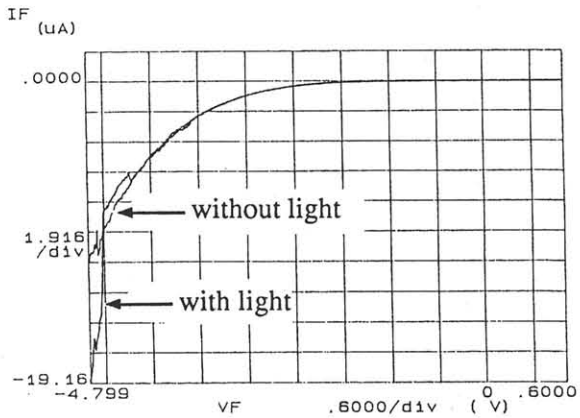
(b) VJFET I-V curve

Figure.2 The individual PIN-VJFET characteristics

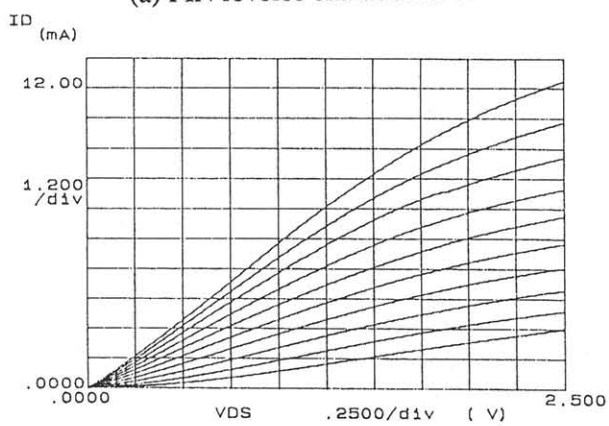
characteristics since it has a large channel depth(grating opening) larger than 5μm and a large gate parasitic series resistance.

To improve the VJFET characteristics, small grating period(3μm) and W insertion between SiO_2 and p-GaAs are used. The first epitaxial layers are the same as in the case of the previous VJFET but p-GaAs is 0.1μm in this case. The sputtered 50/200nm W/SiO_2 were successively deposited. Then unmasked area of SiO_2 is removed by reactive ion etching(RIE). AZ-5214 photoresist is used for the mask material. W is removed by CF_4 and H_2 mixing gases. After the removal of W, RIE is continued to etch GaAs using CCl_2F_2 and H_2 mixing gases. And then the protruded W on the etched surface was removed by dipping in hot H_2O_2 for about 10 sec. Then the second MOCVD epitaxial layers of n^--GaAs/n^+-GaAs are grown. Next SiO_2 etching by 6:1 BOE is followed for opening PIN area. For ohmic contact AuGe/Ni/Au was evaporated on the drain, the source, and the W gate contact areas. Rapid thermal annealing(30sec at 370°C) is performed and W in PIN opening area is removed by dipping in hot H_2O_2.

The individual modified VJFET characteristics is shown in figure 3. The VJFET characteirstics is im-



(a) PIN reverse characteristics



(b) modifed VJFET I-V curve

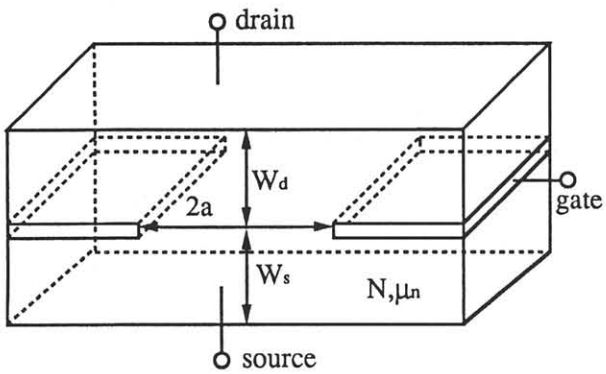
Figure.3 The modified PIN-VJFET characteristics

proved but the PIN junction characteristics is degraded. This should be improved to have a satisfactory PIN operation. Reactive ion etching (RIE) of SiO_2, W by $CF_4 + H_2$ and GaAs by $CCl_2F_2 + H_2$ are done to prevent the undercut in etching. The remaining processes are the same as the above VJFET.

III. Results and Discussions

The VJFET maximum transconductance is about $1mS/(30\mu m)^2$ and for the modified one, $1mS/(10\mu m)^2$ is obtained.

In the fabrication steps the p-type dopant affects the 2nd epitaxially grown lightly doped or undoped n-layer. The 2nd epitaxially grown layer may be fully compensated by p-type dopants if the dopants have large vapor pressure like Zn. Thus the carbon was intrinsically doped by reducing V/III elemental ratio to nearly 1~2. The morphology was good in this ratio but hole carrier concentration is difficult to control. Only the hole carrier concentration ranging between 1×10^{17} and $1\times10^{18}cm^{-3}$ is obtained. Thus some metal should be used to reduce the gate series resistance . W forms satisfactory ohmic contact to p-GaAs. But in the processing steps, W degrades p-n junction characteristics so it must be carefully treated. W protrusion and the edge roughness affect the p-n jnction characteristics. The 2nd epitaxial layer thickness in the active transistor area is easily calculated by the principle that on SiO_2 Ga source freely migrate about 100μm and the growing occurs only when the source reaches the exposed GaAs region. Also the VJFET in this case does not saturate. If it saturates the saturation will be due to the bulk velocity saturation which occurs when the channel depth(grating opening)



W_s : 1st epi layer thickness of n^- GaAs
W_d : 2nd epi layer thickness of n^- GaAs
Z : total channel width
V_{bi}: built-in potential
N : electron concentration of n^--GaAs layer
μ_n : mobility of electron in n^--GaAs layer

Figure.4 Parameters for VJFET model

is large enough so that pinch-off can not take place. If the pinch-off could take place by small channel depth, the dominant mechanism is space charge limited current. Thus drain current I_{DS} will be modeled analytically as follows[3]. From the figure 4 we can see that, before saturation, I_{DS} is given as follows.

$$I_{DS} = 2qN'\mu_n \frac{V_{DS}}{W_s+W_d}\left(a - \sqrt{\frac{2\varepsilon}{qN'}(V_{bi}-V_{GS}+V_{DS})}\right)\cdot Z$$

where

$$N' = \frac{2\pi^2 V_T \varepsilon}{q(W_S+W_D)^2} + N \,,\; V_T = \frac{kT}{q}$$

After the saturation is reached, we have

$$I_{DS} = 2q\left\{ N' + \frac{2V_{DS}\varepsilon}{q(W_s+W_d)^2} \right\}\cdot v_s \cdot \left(a - \sqrt{\frac{2\varepsilon}{qN'}(V_{bi}-V_{GS}+V_{DS,sat})}\right)\cdot Z$$

In the above, v_s is the electron saturation velocity. Here, knee voltage is determined by the drain-source parasitic resistances. $V_{DS,sat} = E_s(W_s + W_d)$, where E_s is the carrier velocity saturation field.

IV. Conclusion

In this paper we have proposed, fabricated and analyzed the integrated PIN-VJFET structure. This will be useful in implementing vertical type OEICs for photodetection and image sensing, etc. The VJFET is improved by W layer deposition on p-GaAs but PIN junction characteristics should be improved.

V. Acknowledgments

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VI. References

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