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Complementary InAs-Channel and GaSb-Channel Quantum Well Heterojunction Field-Effect Transistors

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We report on the fabrication and characterization of vertically integrated InAs n-channel Heterojunction FETs (HFETs) and GaSb p-channel HFETs based on a $(Al_{.5}Ga_{.5})Sb/InAs/(Al_{.5}Ga_{.5})Sb/GaSb/(Al_{.5}Ga_{.5})Sb$ double quantum well heterostructure grown by molecular beam epitaxy (MBE). The operation of both p- and n-channel HFETs fabricated on the double quantum well heterostructure is demonstrated for the first time. Vertically integrated 2μm gate length GaSb p-channel HFET and 1.2μm gate length InAs n-channel HFETs showed decent I-V characteristics with maximum transconductances of 19mS/mm and 88mS/mm at 77K, respectively.

I.INTRODUCTION

Heterostructures of antimonides are intersting system in both physics[1][2] and bandgap engineering point of view. InAs/(AlGa)Sb heterostructures have advantages of high low-field mobility[3], high-lying satellite valleys, deep quantum well and are suitable for high performance InAs channel field-effect transistors [4][5][6]. GaSb/(AlGa)Sb heterostructures, on the other hand, is suitable for high performance GaSb channel MODFETs [7]. Both types of high performance HFETs are based on antimonide heterostructures with lattice mismatch of 1.3% maximum. Vertical combination of the high performance p- and n-HFTs would lead to a complementary heterojunction FET circuitry which would outperform complementary AlGaAs/(InGa)As HFETs[8]-[9]. We have investigated the growth and fabrication of both p- and n-channel HFETs based on various $(Al_{.5}Ga_{.5})Sb/InAs/$ $(Al_{.5}Ga_{.5})Sb/GaSb/(Al_{.5}Ga_{.5})Sb$ double quantum well heterostructures. The structural and process scheme dependences on the electrical characteristics of the both types of HFETs were investigated.

II. STRUCTURAL CONSIDERATIONS

The designed heterostructure consists of InAs/AlGaSb heterojunction on top of the GaSb/AlGaSb heterojunction as shown in Fig.1. We have decided to investigate vertically integrated structure with InAs well on top of the GsSb well for the following reasons. (i) Non-alloyed ohmic contact to n-channel is possible, whereas alloying is necessary to make contacts to GaSb p-channel layer. In the proposed structure, one can make alloyed ohmic contact to the p-channel layer after stripping off the n-channel layer under the gate electrode. However, if the oder is reversed, alloyed ohmic contacts contact to both channels. (ii) In the proposed structure, one can make use of the high selectivity in the etching rate of AlGaSb to InAs, thereby making the total process uniform and reliable.

The schematic energyband diagrams under the gate regions of both p- and n-channel HFETs are shown in Fig.2(a) and Fig.2(b).

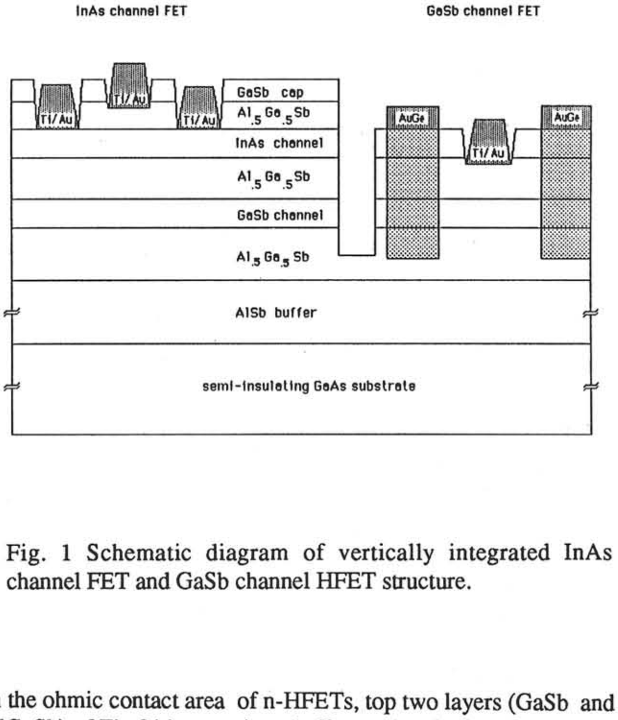


Fig. 1 Schematic diagram of vertically integrated InAs channel FET and GaSb channel HFET structure.

In the ohmic contact area of n-HFETs, top two layers (GaSb and AlGaSb) of Fig.2(a) are stripped off to make ohmic contact to the InAs layer directly. In the ohmic contact region of the p-HFETs, the same procedure as above n-HFET contact region is performed followed by the alloy metal deposition and alloying. Of course this process should precede the non-alloyed ohmic and Schottky metal deposition of both types of HFETs. There remain design issues to be solved such as optimization of doping and thickness of the AlGaSb layer between the two channels. Also, integration of high performance p- and n-channel "enhancement" HFETs is necessary for the advanced complementary circuit applications. But, main purpose of this report is to demonstrate the feasibility of the integrated complementary HFETs based on antimonides and to solve some of the design issues to be overcome eventually.

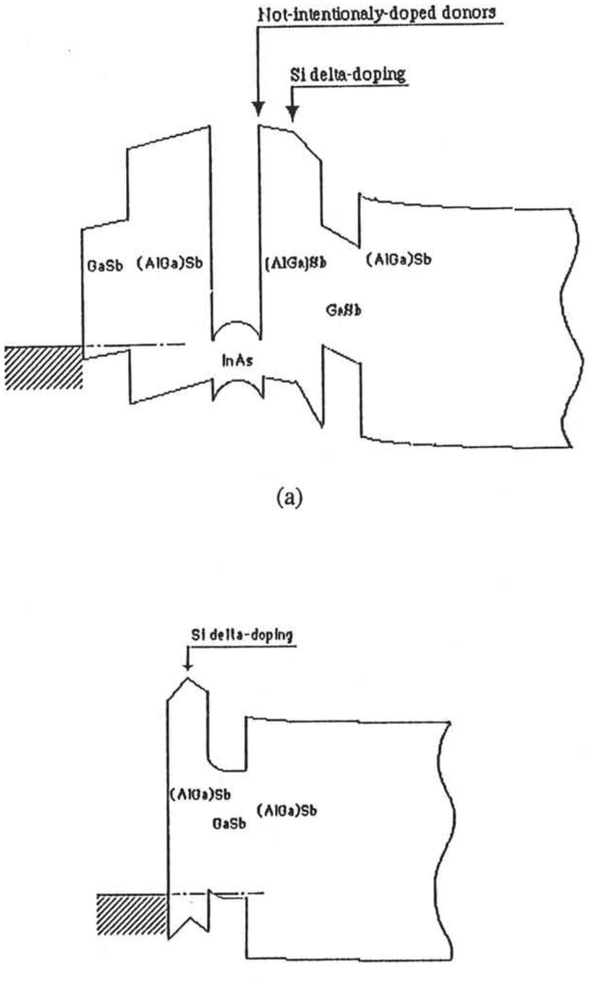


Fig.2 Schematic Energy Band Diagrams of (a) an InAs Heterojunction FET and (b) a GaSb Heterojunction HFET (after gate recess etching).

III. FABRICATION

The heterostructure of the devices consists of 2μm of AlSb buffer layers followed by 2000Å of GaAs buffer layer grown on undoped GaAs substrates, 2000Å of $(Al_{.5}Ga_{.5})Sb$ bottom barrier layer, 150Å of GaSb, 200Å of $(Al_{.5}Ga_{.5})Sb$ layer, 150 Å of InAs, 150 Å of $(Al_{.5}Ga_{.5})Sb$, and 100 Å of GaSb cap layer. $4 \times 10^{12} cm^{-2}$ of silicon atoms were delta-doped in the middle of the $(Al_{.5}Ga_{.5})Sb$ layer which separates InAs and GaSb channels in order to provide holes to the GaSb channel. This doping was intended to serve for three purposes: (i) to provide holes to the GaSb channel, (ii) to ameliorate the ohmic contact to the p-channel, (iii) and to increase the threshold voltage of the n-HFET by compensating the not-intentionary-doped donors near the InAs/AlGaSb interface[3][6]. Surface layers of the p-channel FET region were selectively etched down to the upper interface of the InAs channel. Ohmic contacts to the p-channel HFETs were done by deposition and alloying of AuGe. Surface InAs layer helps to obtain low contact resistance to the GaSb channel. Gate recess etching was carefully done in order to etch-off $(Al_{.5}Ga_{.5})Sb$ surface layer which contains large amount of not-intentionally-doped donors in (AlGa)Sb layer near the InAs interface. Ohmic contact to the n-channel HFET were done by non-alloyed ohmic contact using Ti/Au.

IV. INITIAL RESULTS

The distinctive buried p-HFET characteristics dependence on the process sequence were observed. When the surface InAs is completely removed, the ohmic contacts to the p-channel becomes non-ideal even though the AlGaSb barrier layer is doped with silicon acceptors. When the InAs cap layer for the p-HFET is left, the ohmic contact to the p-channel gets better. Gate-to-source resistance was worse for the case without InAs layer than the case with InAs layer. Fig.3 shows the I-V characteristic of a GaSb p-channel HFET with InAs cap layer on top of the AlGaSb barrier.

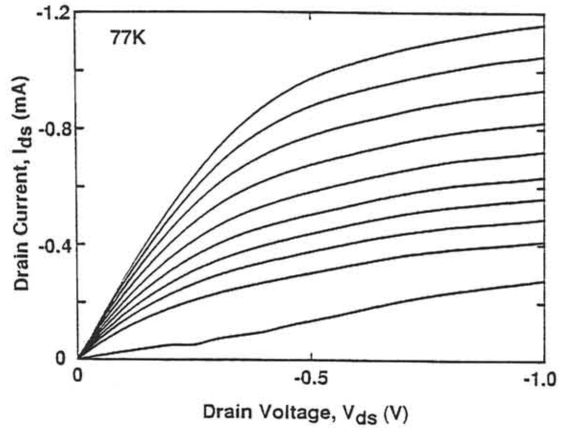
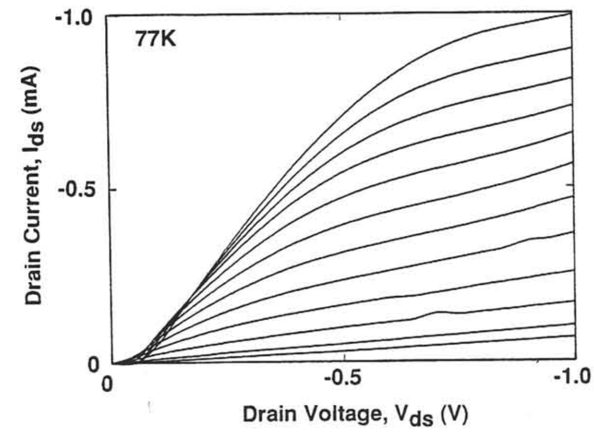


Fig. 3. I_{ds}-V_{ds} characteristics of a GaSb/(AlGa)Sb p-channel HFET in a vertically integrated complementary structure. V_{gs}=0.5 to -0.4V by -0.1V step.

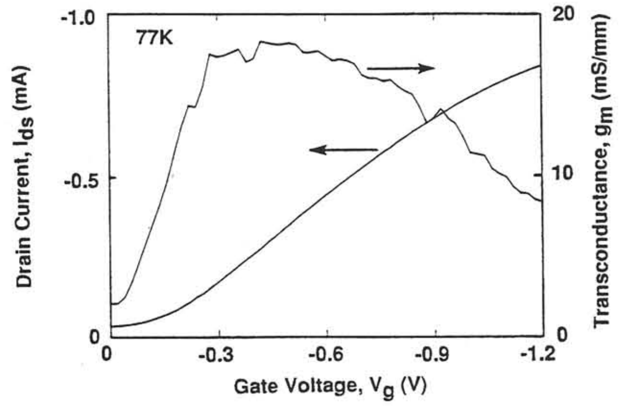
Decent pinch-off characteristics with the maximum transconductance of 20mS/mm at 77K was obtained. However, one notices that the operation is in depletion mode. Obviously enhancement p-FET is needed for the complementary circuit applications. In the next section, enhancement mode p-channel HFET is described.

V. RESULTS OF AN IMPROVED STRUCTURE

As a second step, we have investigated otherwise the same heterostructure as what was explained above but without silicon doping in the AlGaSb barrier layer between channels. As expected, the Hall measurement for the two dimensional hole gas were impossible without gate control, i.e., if the surface InAs layer is left for the Hall sample, one measures parallel conduction in the InAs layer, and if the InAs layer is removed, the two-dimensional-hole gas will not be induced. Hall-effect measurements of the two-dimensional-electron-gas formed on top of the p-HFET structure has been done using non-alloyed ohmic contact: mobility and sheet carrier concentration were 12900 $cm^2/Vsec$ and 2.05×10^{12} cm^{-2} at 77K respectively. Good pinch-off characteristics were observed for both n- and p-channel HFETs vertically integrated on the same wafer as can be seen in Fig.4 and Fig.5. Typical transconductances of the InAs channel HFETs and GaSb channel HFETs were 88mS/mm and 19mS/mm, respectively at 77K. This is the first demonstration of



(a)



(b)

Fig.4 Current-Voltage characteristics of an enhancement mode GaSb/(AlGa)Sb p-channel HFET in a vertically integrated complementary structure. (a) I_{ds} versus V_{ds} curve with V_{gs}=0 to -1.2V by -0.1V step. (b) I_{ds}, transconductance versus V_{gs} curves. The channel length and width are 2μm and 50μm respectively.

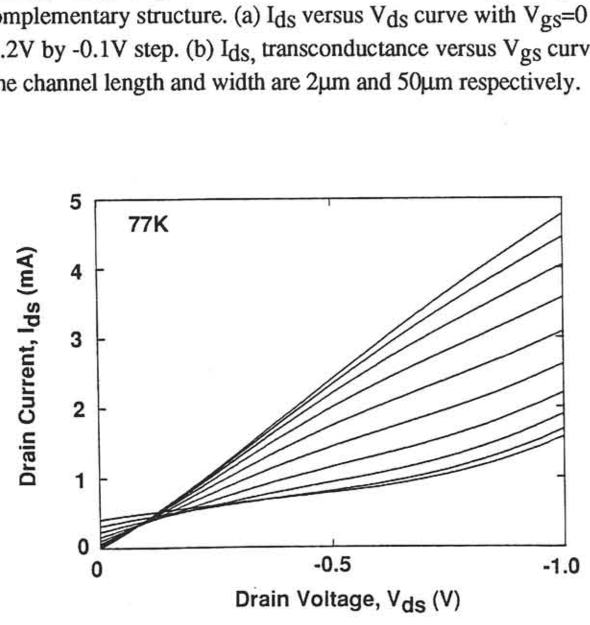


Fig.5 I_{ds}-V_{ds} characteristics of a InAs/(AlGa)Sb n-channel HFET in a vertically integrated complementary structure. V_{gs}=-0.8 to 0.1V by 0.1V step.The channel length and width are 1.2μm and 50μm respectively.

monolithically integrated InAs channel HFETs and GaSb channel HFETs. The p-HFETs in this case operate in enhancement mode as expected. The next step is to make the n-HFETs to work also in enhancement mode. Although the structure is not optimized yet, the present results clearly show the feasibility of the complementary InAs channel and GaSb channel heterostructure HFETs.

VI. CONCLUSIONS

The operation of both GaSb/(AlGa)Sb p-HFETs and InAs/(AlGa)Sb n-HFETs fabricated on a double quantum well heterostructure is demonstrated for the first time. Vertically integrated 2μm gate length GaSb-channel FET and 1.2μm gate length InAs n-channel FET showed decent I-V characteristics with maximum transconductances of 19mS/mm and 88mS/mm at 77K, respectively.

VII. ACKNOWLEDGMENTS

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