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A Super Low-Noise AlGaAs/InGaAs/GaAs DC-HFET with 0.15 µm Gate-Length

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A DC-HFET has been developed using an AlGaAs/InGaAs/GaAs pseudomorphic system which has a superior electron confinement effect compared with an AlGaAs/GaAs system. An excellent NFmin of 0.65dB and a Ga of 11.3dB were realized at 12GHz (Ids=18mA, Vds=2V). The gm at Ids=10mA was 385mS/mm and gm_{max} reached 570mS/mm (Ids=50mA). A promising DC-HFET structure was also proposed to further improve characteristics. It incorporates both an undoped GaAs barrier layer and a self-aligned n⁺ layer formed by ion-implantation.

1. INTRODUCTION

It used to be widely believed that HEMTs had superior DC and RF characteristics (low-noise performance, etc.) to those of MESFETs, because of a high electron mobility in the channel. Hasegawa¹⁻³) suggested that the transconductance (gm) of HEMT was superior to that of MESFET, due mainly to a thin gate depletion layer caused by high doping. He also proposed that the gm of MESFET with a highly-doped channel layer could be raised above that of HEMT. A year later, a DC-HFET (Doped Channel Hetero FET) with a highly-doped channel layer was developed using an AlGaAs/GaAs system⁴). Because of its excellent current drivability and large breakdown voltage, it has been widely investigated for ultra high speed devices⁵). However, there have been few reports the low-noise performance on or of FETs using electrical characteristics⁶⁾ an AlGaAs/InGaAs/GaAs pseudomorphic system with a superior electron confinement effect compared with the AlGaAs/GaAs system.

This paper describes, for the first time, preliminary low noise characteristics of a 0.15_{μ} m gate AlGaAs/InGaAs/GaAs DC-HFET, and a promising device structure to further improve the characteristics.

2. DEVICE STRUCTURE AND FABRICATION PROCESS

Figure 1 shows an AlGaAs/InGaAs/GaAs DC-HFET structure. The wafer for the DC-HFET consists of an undoped GaAs buffer layer, an n-InGaAs channel layer ($n=2.5\times10^{18}$ cm⁻³, d=100Å, In mole fraction 0.15), an n-AlGaAs barrier layer and an n-GaAs cap layer. The wafer for the pseudomorphic HEMT, which was fabricated in order to compare the device characteristics with the DC-HFET, has an undoped InGaAs channel (d=150Å, In mole fraction 0.15), instead of an n-InGaAs channel for the DC-HFET. These wafers were grown by the MBE method at a GaAs substrate temperature of about 510°C.

The electron mobility of the DC-HFET's and the pseudomorphic HEMT's wafer, obtained from Hall mesurement, were about $2000 \text{cm}^2/\text{V} \cdot \text{sec}$ and $5000 \text{cm}^2/\text{V} \cdot \text{sec}$ at 300K, and about $2500 \text{cm}^2/\text{V} \cdot \text{sec}$ and $15000 \text{cm}^2/\text{V} \cdot \text{sec}$ at 77K, respectively.



Fig.1 AlGaAs/InGaAs/GaAs DC-HFET structure

The device fabrication process is fundamentally based on a standard recessed-gate FET technology, which is briefly described as follows: After device isolation through mesa etching, alloyed AuGe/Ni/Au metal was used for the source and drain ohmic contacts. Then the electron-beam lithography technique using an EBR-9/PMMA double-layered resist system was employed for T-shaped gate pattern fabrication. The T-shaped gate electrode was fabricated,



Fig.2 Cross-sectional SEM photograph of a $0.15 \,\mu$ m gate device

by wet-recess etching, Ti/Al evaporation and lift-off of the gate metal. Figure 2 shows the cross-sectional SEM photograph of a 0.15μ m gate device with a gate width (Wg) of 200μ m.

3. DEVICE CHARACTERISTICS

Figure 3 shows the gm and drain current (Ids) as a function of the gate voltage (Vgs) of the DC-HFET. For the DC-HFET, a rapid increase in gm in the low Ids region was obtained, which is very important for low-noise operation, and a gm of 385mS/mm was achieved with a Wg of 200µm and a Ids of 10mA. The maxium gm (gmmax) reached 570mS/mm at a Ids of 50mA. On the other hand, for the pseudomorphic HEMT, a gm of 375mS/mm at a Ids of 10mA and a gmmax of 550mA/mm at a lds of 40mA were obtained. These results show that the DC-HFET is superior the pseudomorphic HEMT in terms of gm. to Figure 4 shows a NF and a Ga at 12GHz for the DC-HFET and the pseudomorphic HEMT. An excellent minimum NF (NFmin) of 0.65dB was obtained for the DC-HFET at a Ids of 18mA, and the NF remained less than 0.8dB throughout a large Ids region (10~30mA). This weak dependance of NF on Ids is very similar to that found in pseudomorphic HEMT. However, compared to the pseudomorphic HEMT, the NFmin was inferior by approximately 0.15dB, and the difference in the NF became large in the low Ids region. A Ga of 11.3dB was obtained for the DC-HFET. The Ga became larger in the high Ids region and smaller the low Ids region than that of in the pseudomorphic HEMT.

Figure 5 shows the NF and Ga of DC-HFET as a function of frequency. The Ga maintains an almost linear correlation with the logarithm of

frequency. The NF has a weak dependence on frequency, as in the case of HEMT. A NF of 1.05dB and a Ga of 9.5dB were obtained, even at 18GHz.

The DC-HFET had superior gm, but inferior



Fig.3 gm and Ids as a function of Vgs



Fig.4 NF and Ga at 12GHz of DC-HFET and pseudomorphic HEMT



Fig.5 NF and Ga of DC-HFET as a function of frequency

NF to that of the pseudomorphic HEMT. We investigated the cause of the above results from the point of view of an equivalent circuit parameter. Table 1 shows values of the equivalent circuit parameters which were extracted from S-parameters. As shown in Table 1, the gm, gate-source capacitance (Cgs), source resistance (Rs) and gate resistance (Rg) of the DC-HFET were larger than those of the pseudomorphic HEMT. Other parameters had nearly the same values. As for the gm, this result agrees with the above mentioned experimental result. The difference in the Rg value is attributed to error in the gate fabrication process. These results indicate that the inferior NF for the DC-HFET is mainly caused by larger Cgs and Rs, which originate in the wafer structure.

4. NEW DEVICE STRUCTURE

A promising device structure to further improve the characteristics, as shown in Figure 6, was designed by introducing both an undoped GaAs barrier layer and a self-aligned n+ layer formed by ion-implantation, because these can reduce not only Cgs but also the series resistance between the channel and the cap layers. However, this structure requires a new post-implantation annealing technique which can minimize decreases in electron density of the channel in the annealed hetero-structure wafers, because deep level traps, such as SA center7), are generated relatively easily during the annealing process.

Figure 7 shows the reduction of sheet carrier concentration of the wafer with the n-InGaAs channel layer as a function of annealing temperature. We have developed a rapid thermal annealing technique using SiN caps formed by ECR-PCVD, which can suppress such decreases down to about 6% at an annealing temperature of about 900°. The sheet resistance of the n-InGaAs layer was also recovered up to the as grown level. Furthermore, this annealing characteristic is convenient for device fabrication because the optimum temperature agrees with the activation conditions of the n⁺ layer.

Table	1	Values	of	the	equivalent	circuit
		paramet	ers			

equivalent circuit parameter	DC-HFET	pseudomorphic HEMT	
gm (mS)	143.2	128.5	
Cgs (fF)	340	302	
Cgd (fF)	22	21	
Cds (fF)	139	133	
Rs (Ω)	2.5	1.8	
Rd (Ω)	3.6	2.8	
Rg (<u></u> ቢ)	1.15	0.9	



Fig.6 New DC-HFET structure







5. SUMMARY

We have successfully developed a preliminary low-noise AlGaAs/InGaAs/GaAs DC-HFET with a 0.15_{μ} m gate length. An excellent NFmin of 0.65dB and a Ga of 11.3dB were realized at 12GHz (Ids=18mA, Vds=2V). The gm at 10mA was 385mS/mm and gm_{max} reached 570mS/mm (Ids=50mA). The device structure designed by introducing both an undoped GaAs barrier layer and a self-aligned n⁺ layer formed by ion-implantation promises to enable further improvement of the characteristics.

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