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The Room Temperature Characteristics of GaAs δ-Doped Superlattice Switching Transistor

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In this paper, a new functional GaAs switching transistor is demonstrated. A sawtooth δ–Doped superlattice is introduced between anode and cathode. Holes, created by the avalanche multiplications near the metal–semiconductor (M–S) junction, play an important role in the transport properties. An attractive S–shaped negative differential resistance (NDR) phenomenon in the experimental current–voltage characteristics is observed. Furthermore, with proper operation of the third electrode, gate, the studied structure performs a controllable switching characteristics.

1. INTRODUCTION

Recently, for being used on the high frequency oscillators and microwave circuits, the N–shaped or S–shaped negative–differential–resistance (NDR) devices have attracted great attentions in circuit applications. However, quite a few three–terminal switching devices with S–shaped NDR have ever been reported. In spite of that, with the increasing improvement of semiconductor growth technologies, e.g., molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD) etc, it becomes possible to locate impurity doping profile at an atomic layer. Therefore, a new artificial doping technology, the monolayer doping or δ–doping, has been successfully developed.[1] In addition, Schubert et al. have achieved the sawtooth–doping–superlattice (SDS) structure[2-6] based on the doping superlattice concept of Esaki et al.[7] and the δ–doping method of Wood et al.[1] The SDS is fabricated by altering periodic n– and p–type dopants onto semiconductor within a considerably short length scale period and causes a great potential modulation in the band structure. With a long period such as 600Å, the SDS structure exhibits an S–shaped NDR phenomenon.[5] In this paper, we propose a new three–terminal–controlled GaAs switching device in which a double SDS structure with two different δ–doping sheets and a metal–semiconductor (M–S) structure are employed. In the proposed structure, holes are generated from the avalanche breakdown near the M–S junction and accumulated at the valence band maxima of the zigzag quantum wells. It causes a potential redistribution in the band structure. As a result, the studied device exhibits a controlled S–shaped NDR performance at room temperature.

2. EXPERIMENTS

The structure studied was grown on a (100)–oriented n^+–GaAs substrate by MBE. The details of substrate preparation and layers growth were described elsewhere.[8-9] The growth sequence included a 0.7 μm Si–doped GaAs ($n=1\times10^{18}$ cm^{-3}) buffer layer, SDS1, SDS2, and a 0.3 μm Be–doped GaAs ($p=1\times10^{17}$ cm^{-3}) cap layer. The SDS1 was composed of 3–period $\delta(n^+)$–i–$\delta(p^+)$–i superlattice with $\delta(n^+)=\delta(p^+)=1\times10^{13}$ cm^{-2} and i=300Å while the SDS2 was 3–period $\delta(n^+)$–i–$\delta(p^+)$–i superlattice with $\delta(n^+)=\delta(p^+)=1\times10^{12}$ cm^{-2} and i=300Å. The growth temperature of the GaAs host material was Ts=580°C which was reduced to 500°C when the delta–doping layers were growing. After the epitaxial growth finishing, the ohmic contact was then formed to the cathode (K) by the deposition of AuGe metal on the bottom n^+–GaAs layer. Besides, the Schottky contacts were employed to anode (A) by the deposition of Au metal on the top p–GaAs layer. Then, the wafer was etched into the n^+–GaAs buffer layer using a wet chemical etching solution ($3NH_4OH:1H_2O_2:50H_2O$, 300K). The schematic illustration of studied device is depicted in Fig.1.

3. RESULTS AND DISCUSSIONS

Fig.2 shows the energy band diagrams of studied devices. As shown in Figs.2 (a) and (b), due to the sufficient barrier height and width, the conducting current originating from the thermionic emission or tunneling is so small as to be neglected when the device is operated under zero bias or a small anode–cathode voltage V_{AK}. As V_{AK} is increased further, at some voltage Vs, an avalanche

multiplications near the metal–semiconductor (M–S) junction occurs. Then, holes, created by the avalanche multiplications, are accumulated at the valence band maxima, as shown in Fig.2 (c). In figure 2(c), the solid lines describe that the strong electrical field just causes the avalanche breakdown at M–S junction, but holes don't be transported into the sawtooth potential wells yet. Moreover, the dashed lines interpret that the holes trapped in zigzag quantum wells and yield the collapse of potential barriers due to the screening effect of acceptors. This causes the potential redistribution in SDS regions and performs an S–shaped NDR in current–voltage (I–V) characteristics at room temperature. The total conducting current will then rapidly increase because the potential barrier height for electrons injection are lowered substantially. The experimental I–V characteristics between anode and cathode at room temperature is shown in Fig.3 (a). As we expected, the S–shaped NDR is observed at 300K. When V_{AK} is small, the conduction current can be neglected. At some V_{AK} voltage, Vs, the sufficiently electrical field causes the avalanche multiplications and yields an onset of switching phenomenon. The switching parameters are Vs=8.0V, V_H=5.7V, I_H=1.0mA, and voltage control ratio V_S/V_H=1.42, respectively.

Fig.1(b) depicts the schematic cross section of the structure studied for three–terminal operation. Obviously, by using the gate electrode through the n^+–GaAs buffer layer, it is a series composition of two–terminal structure as shown in Fig.1 (a). The application of a bias V_{GK} at gate electrode can control the initial off–state switching voltage Vs across the anode and cathode regions. As illustrated by long–dotted line in Fig.2 (d), once a negative V_{GK} voltage is applied, the SDS region is biased under an additional voltage drop with a magnitude of V_{GK} over the gate floated condition. The employment of negative V_{GK} voltage causes an effective enhancement on carrier transport in SDS A region and the conduction current, through anode–gate loop, is increased simultaneously. So, the initial off–state switching voltage Vs is expected to be lower than that at gate floated condition.

Figs.3 (b) and (c) shows the experimental I–V characteristics of the studied device under three–terminal operation. Fig.3 (b) shows the I–V characteristics between anode and cathode with the negative control voltages V_{GK}. In accordance to our prediction, the initial off–state switching voltage Vs is decreased with increasing the magnitude of the applied negative gate voltage V_{GK}. In addition, Fig.3 (c) shows the I–V characteristics between anode and cathode with the negative control current I_G. When the applied negative current I_G is increased, the magnitude of the negative voltage V_{GK} is also increased. As mentioned above, it causes an increment of anode current I_A under the same anode–to–cathode bias V_{AK}.

4. CONCLUSIONS

We have demonstrated a new three–terminal–controlled GaAs switching device with double SDS structures. The studied device exhibits an interesting S–shaped NDR performance. The NDR phenomenon is attributed to the avalanche multiplications at M–S interface and the potential redistribution in SDS. Furthermore, the band structure and carrier transport properties can be adjusted effectively when the third electrode, i.e., gate, is employed. The facility of three–terminal operation provides the wide and flexible application capability. Consequently, with an appropriate design of the structural parameters, e.g., the delta doping density and the SDS number etc, the proposed structure exhibits good potential for switching circuit and multiple–valued logic circuit applications.

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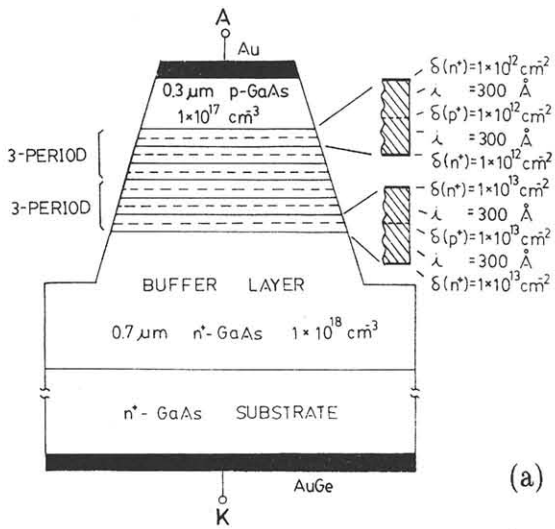
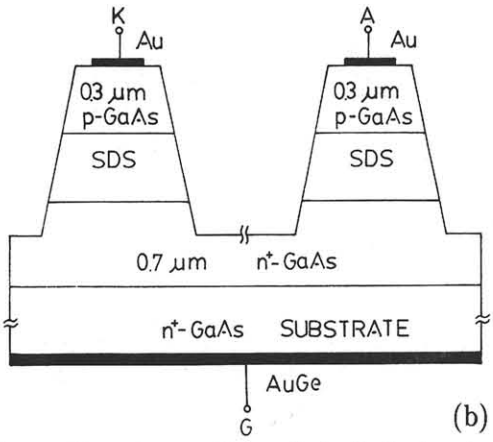
5. REFERENCES

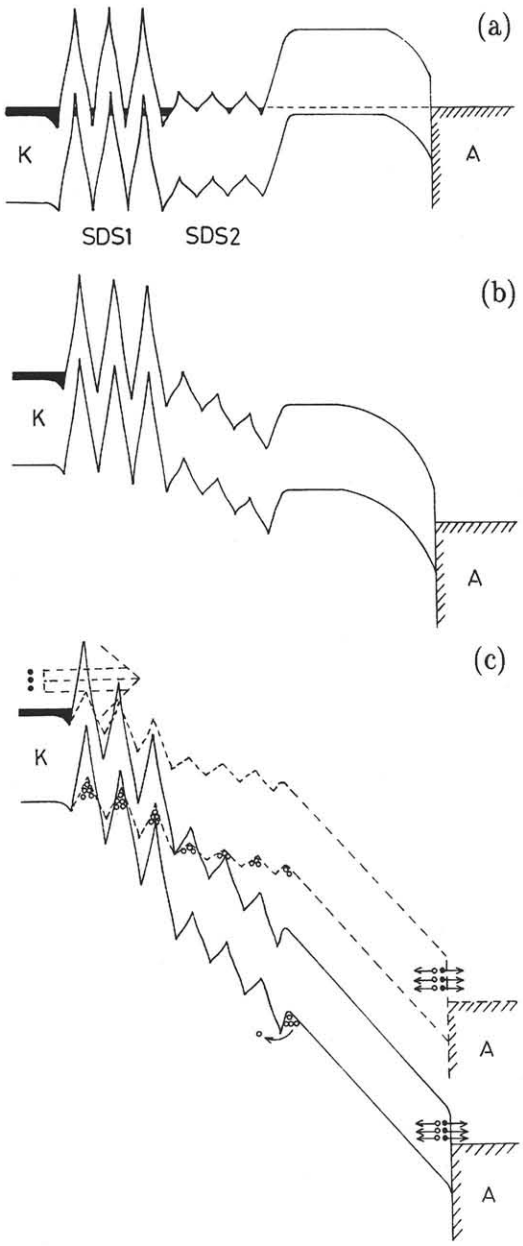
1) C.E.C. Wood, G. Metze, J. Berry and L.F. Eastman : J. Appl. Phys. 51 (1980) 383
2) E.F. Schubert, A. Fischer and K. Ploog : Electron Lett. 21 (1985) 411
3) E.F. Schubert, A. Fischer, Y. Horikoshi and K. Ploog : Appl. Phys. Lett. 47 (1985) 219.
4) E.F. Schubert, Y. Horikoshi and K. Ploog : Phys. Rev. B32 (1985) 1085
5) E.F. Schubert, J.E. Cunningham and W.T. Tsang : Appl. Phys. 51 (1987) 817.
6) E.F. Schubert, B. Ullrich, T.D. Harris and J.E. Cunningham : Phys. Rev. B38 (1988) 835.
7) L. Esaki and R. Tsu : IBM J. Rev. Dev. 14 (1970) 61.
8) W.C. Liu, R.L. Wang, W.S. Lour, C.Y. Sun and C.C. Hong : Jpn. J. Appl. Phys. 29 (1990) L7.
9) W.C. Liu, and C.Y. Sun : Jpn. J. Appl. Phys. 30 (1991) 635.

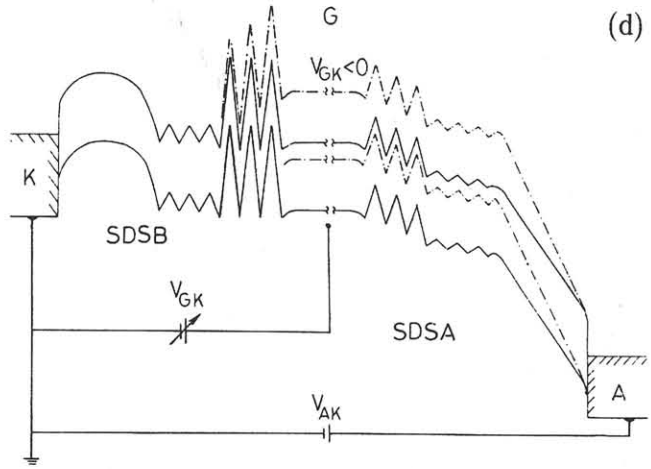


(a)

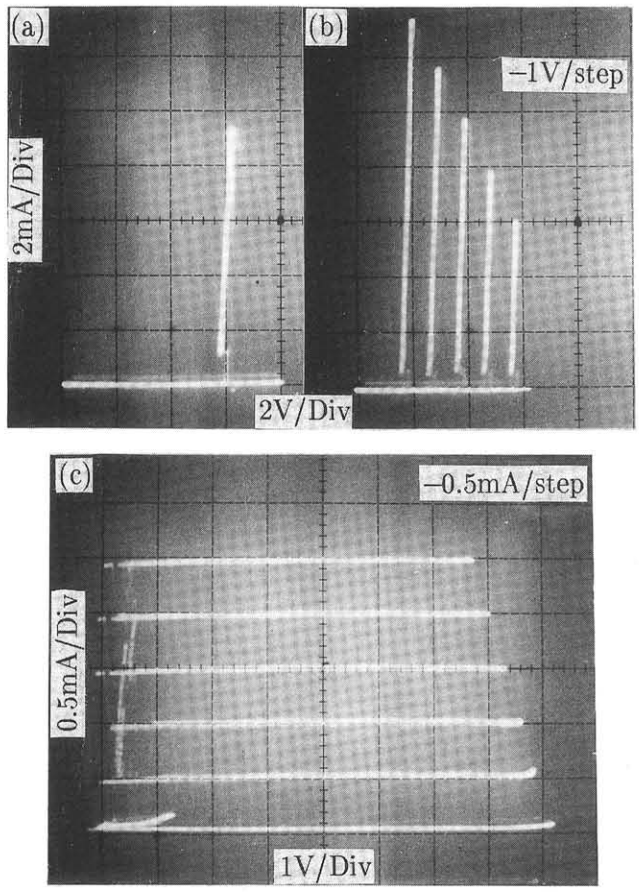


The schematic cross section of studied structure for (a) two terminal(b) three terminal operation





The corresponding energy band diagrams of the studied devices at (a) zero bias (b) a small positive bias (c) increased positive bias, the zigzag potential barriers redistribute after the avalanche breakdown process occurring at the M–S junction (d) three–terminal operation with negative VGK voltage.



The room temperature I–V characteristics of the studied devices under (a) two–terminal operation (b) three–terminal operation with applied negative VGK bias (c) three–terminal operation with applied negative IG current.