Low Temperature Operation of Polycrystalline Silicon Thin Film Transistors


Research Center for Integrated Systems, Hiroshima University
1-4-2 Kagamiyama, Higashi-Hiroshima 724, Japan

*Palo Alto Research Center, Xerox Co.
3333 Coyote Hill Road, Palo Alto, CA 94304, U.S.A.

The influences of the grain boundary traps on poly-Si TFT device characteristics were evaluated in detail by examining the low temperature device characteristics. It was found that the threshold voltage significantly increases and the field effect mobility considerably decreases at the low temperature because the influences of the grain boundary traps become more pronounced. As a result, the drain current is strikingly reduced when the temperature is decreased. Meanwhile, the kink effect is suppressed at the low temperature due to the increased influences of the grain boundary traps. The hydrogenation treatment mitigated the drain current reduction at the low temperature and enhanced the kink effect.

1. INTRODUCTION

In recent years, polycrystalline silicon thin film transistors (poly-Si TFTs) have attracted much attention for the various applications to the large area electronics and three-dimensional LSIs. However, its operation mechanism is not always fully understood due to the complexity of the grain boundary trap properties. The device characteristics are significantly influenced by the grain boundary traps in poly-Si TFTs. In addition, poly-Si TFTs suffer from the harmful kink effect which deteriorates the circuit performance. Therefore, it is very important in poly-Si TFT to evaluate the grain boundary trap properties in detail and to elucidate the mechanism of the kink effect. The trap properties and kink effect can be revealed more clearly by measuring the device characteristics decreasing the temperature because the influences of the grain boundary traps and the kink effect become more pronounced in the low temperature. In this paper, we discuss the influences of the grain boundary traps and the kink effect in poly-Si TFT based on the low temperature device characteristics of poly-Si TFT.

2. EXPERIMENTAL

Poly-Si TFTs were fabricated on the oxidized silicon wafer according to the high temperature process where the maximum processing temperature was 950 °C [1]. Both the gate oxide thickness and the poly-Si film thickness were 100 nm. The gate length and the gate width are 20 μm and 50 μm, respectively. The n⁺ poly-Si gate is used for both n-channel and p-channel TFTs. The temperature dependence of poly-Si TFT characteristics was measured in the range of 300 K to 16 K. The hydrogenated TFTs (hydrogenation time tH = 8 hours) were also measured.

3. RESULTS AND DISCUSSION

The typical drain current-drain voltage characteristics of the non-hydrogenated poly-Si TFTs are shown in Fig. 1 where the temperature is changed as a parameter under the constant gate voltage of 10 V. The characteristics show the tendency of a decreasing drain current with decreasing the temperature. This tendency is opposite to that of the temperature dependence for bulk MOSFET. This difference is caused by the grain boundary traps. Figure 2 shows the temperature dependence of threshold voltages. Threshold voltage Vth is defined as the gate voltage where the drain current of 1 nA flows. The threshold voltages of the non-hydrogenated TFTs are significantly increased with decreasing the temperature because the Fermi potential is increased and the influence of the grain boundary traps become more pronounced as shown in Fig. 3. The acceptor-type grain boundary trap plays an important role in n-channel poly-Si TFT [2]. This acceptor-type trap is located in the upper half part of the energy gap. The negatively charged acceptor-type traps are increased when the temperature is decreased as shown in Fig. 3. As a result, the threshold voltage is more significantly increased with decreasing the temperature. The

![Fig. 1 Drain current-drain voltage characteristics of poly-Si TFTs.](image-url)
hydrogenation treatment reduces the acceptor-type trap density and consequently lowers the threshold voltage. The increment of the threshold voltage by decreasing the temperature is also reduced by the hydrogenation treatment. The similar behavior of the threshold voltage is obtained in p-channel poly-Si TFTs, although the threshold voltage is higher than n-channel TFT even after the hydrogenation treatment. The donor-type trap, which is located in the lower half part of the band gap, plays an important role in p-channel TFT. The increased effect of the grain boundary traps in the low temperature can be seen more clearly on the field effect mobility \( \mu_{\text{FE}} \) as shown in Fig. 4. The field effect mobility is monotonously decreased as the temperature is decreased. This is completely different from the case of bulk MOSFET where the field effect mobility is dramatically increased with decreasing the temperature. The decreased field effect mobility of n-channel TFT in the low temperature is due to the increased coulombic scattering by the negatively charged acceptor-type grain boundary traps. The field effect mobility of p-channel TFT shows the considerably different temperature dependence from that of n-channel TFT. It is initially increased due to the reduced phonon scattering inside the grain and then decreased due to the increased coulombic scattering as the temperature is decreased. We can expect from such difference between n-channel and p-channel TFTs that the influences of the grain boundary traps are less in p-channel TFT than in n-channel TFT and hence the donor-type trap density is lower than the acceptor-type trap density. Figure 5 shows the temperature dependence of the subthreshold voltage swing \( S \). The subthreshold voltage swing of n-channel TFT is initially decreased and then increased as the temperature is decreased, while that of p-channel TFT is monotonously decreased like bulk MOSFET. The increase of the subthreshold voltage swing for n-channel in the low temperature is again due to the increased influences of the acceptor-type grain boundary traps.

The kink effect is the harmful effect for poly-Si TFTs because it deteriorates the circuit performance. Figure 6 shows the temperature dependence of the kink coefficient \( K \) which is defined as \( \frac{\partial I_{\text{DS}}}{\partial V_{\text{DS}}} \) in the higher drain voltage region and indicates the susceptibility for the impact ionization. The kink coefficient is decreased with decreasing the temperature in the non-hydrogenated TFTs and is increased by the hydrogenation treatment. The increased kink coefficient is decreased as the temperature is decreased in the hydrogenated n-channel TFT. On the other hand, the kink coefficient on the hydrogenated p-channel TFT is initially increased and then decreased as the temperature is decreased. Figure 7 shows the drain current \( I_{\text{ Dex }} \) dependence of the kink current \( I_{\text{kink}} \). The drain current \( I_{\text{ Dex }} \) is defined as the extrapolated drain current after subtracting the kink current as shown in Fig. 1. As is obvious in Fig. 7, the kink current \( I_{\text{kink}} \) is dramatically decreased in the smaller drain current region. Consequently, the non-hydrogenated TFTs represent
more significant $I_{\text{Dex}}$ dependence of $\Delta I_K$ because the drain current in the non-hydrogenated TFT is much smaller than that in the hydrogenated TFT. Therefore, the decrease of the kink coefficient in the non-hydrogenated TFTs with decreasing the temperature is mainly due to the decrease of the drain current. Meanwhile, the $I_{\text{Dex}}$ dependence of $\Delta I_K$ is not significant in the hydrogenated TFTs because the larger drain current flows. Therefore, the decrease of the kink coefficient in the hydrogenated n-channel TFT with decreasing the temperature as shown in Fig. 6 is due to the decreased impact ionization probability caused by the grain boundary trap. In the hydrogenated p-channel TFT, $\Delta I_K$ represents the similar temperature dependence to the kink coefficient. Thus, it was revealed that the kink effect in poly-Si TFT is suppressed in the lower temperature due to the decrease of the drain current when the grain boundary trap density is higher and the decrease of the impact ionization probability when the grain boundary trap density is lower. The kink effect is rather enhanced with decreasing the temperature when the grain boundary trap density is very low.

4. CONCLUSION

The influence of the grain boundary traps on the poly-Si TFT characteristics are investigated by measuring the poly-Si TFT characteristics in the low temperature. The threshold voltage is increased due to the increased acceptor-type traps in n-channel TFT and the increased donor-type traps in p-channel TFT. The field effect mobility is decreased due to the increased coulombic scattering caused by the grain boundary traps as the temperature is decreased. The kink effect is suppressed owing to the decreased drain current and the decreased impact ionization probability caused by the grain boundary traps in the lower temperature. Thus, it is revealed that the influences of the grain boundary traps become more pronounced in the low temperature.

REFERENCES