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A New Method to Estimate Grain Boundary Trap State Density in Poly-Si TFTs

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A new method of estimating grain boundary trap state density is proposed by modifying Levinson's method. There are two differences between Levinson's and ours. One is the assumption of carrier density to contribute to conduction, and the other is the region of gate voltage used in estimation. The validity of two methods is investigated by device simulation, and it is shown that our method is more accurate than Levinson's method.

1. Introduction

The poly-Si TFT is expected to be used in driving circuits for large-area devices such as image sensors and LC displays. The performance of the poly-Si TFT is strongly influenced by grain boundary traps, so it is important to estimate grain boundary trap state density, N_t. The Levinson's method[1] is widely used for this purpose, and is based on the assumption that the carrier density is uniform over the channel depth t_{ch}. Since this assumption is oversimplified, it is questionable whether N_t derived by Levinson's method is accurate. There were some efforts to modify it, for example by considering the dependence of channel depth in gate voltage[2], but they also assumed uniform carrier distribution.

In this paper, a new method of estimating N_t is proposed by modifying Levinson's method. It assumes that only surface current dominates the total current in the channel. The validity of our method is confirmed by our two-dimensional device simulator for poly-Si TFT[3].

2. Assumption in Levinson's Method

The conduction in poly-Si film can be described by thermionic emission over potential barrier V_B induced at grain boundary. In the Levinson's method, the dependence of V_B in the gate voltage(V_G) is calculated as follows

$$V_B = \frac{qN_t^2 t_{ch}}{8\varepsilon C_0 (V_G - V_{TH})} . \qquad (1)$$

Here, ε is permitivity in Si, and C_0 is capacitance of gate oxide. In this expression, the carrier density is assumed to be uniform over t_{ch} and proportional to the gate voltage. Then N_t is derived from I_D-V_G characteristics.

However, this assumption is far from the actual carrier distribution. Carrier density changes drastically as a function of depth in the channel.

3. New Method to Estimate N_t

We have modified Levinson's method, in which carrier density is treated more accurately. In our method, it is assumed that current near the surface dominates total current in the channel and that drain current is approximated by using carrier density at the surface as

$$I_D \propto n \exp\left(-\frac{qN_t^2}{8\varepsilon n_0 kT}\right) , \qquad (2)$$

where n is free carrier density and n_0 is total (free + trapped) carrier density at surface. The n_0 is not as simple as Levinson's method, but can be calculated by solving the Poisson's equation numerically. Then N_t is evaluated from the gradient of $\ln(\partial I_D/\partial V_G)$ - $1/n_0$ plot instead of $\ln(\partial I_D/\partial V_G)$ - $1/V_G$ used in the Levinson's method.

Our method has two merits. One is that it's free from the indefinite quantity t_{ch} unlike

equation (1). The other is that our method is applicable to low gate voltage region. At rather high voltages, for example above the threshold voltage, carrier conduction isn't influenced only by the grain boundary but also by intragranular resistance. This means that equation (2) is no longer valid. This is explained as follows. At low voltage, the width of depletion region W_g is about a grain size L_{grain}, and most of the drain voltage is applied to the grain boundary ($V_a \simeq V_{gb}$) as indicated in Fig.1(a). But at higher voltages, the depletion region becomes narrow and the voltage drop across the inside of the grain becomes significant as Fig.1(b). Then the effect by intragranular resistance becomes comparable to the grain boundary. Levinson's method is used above the threshold voltage, where its carrier density assumption is valid. This results in inaccuracies in Levinson's method. From above two points, we expect our method to be more accurate.

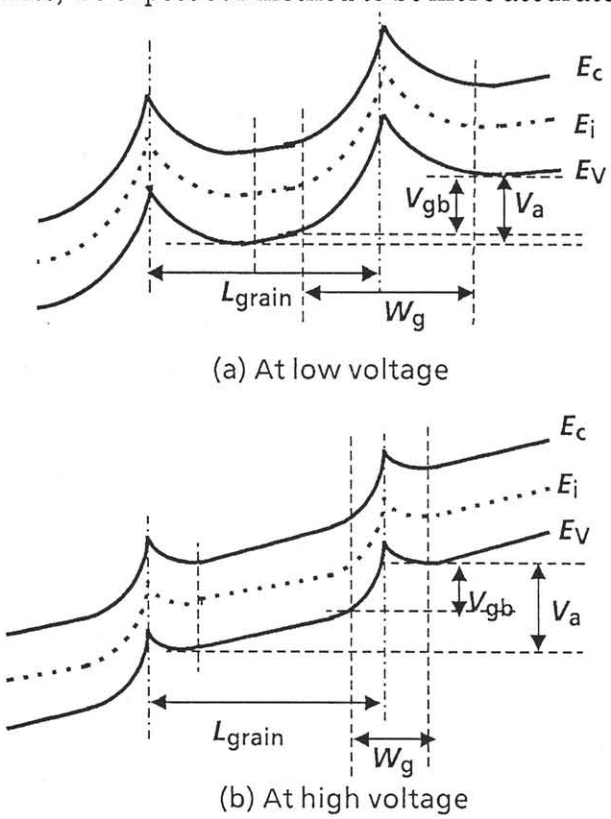

Fig.1. Energy band diagram of poly-Si.
V_a is the total voltage drop across one grain, and V_{gb} is across only grain boundary.

4. Confirmation by Device Simulation

The validity of our method is investigated by our device simulator. It takes account of the effect of grain boundaries using the grain-boundary-trapping model. Since both Levinson's and our method are also based on that model, their validity can be investigated by using our simulator. At first, for a given value of $N_{t_{in}}$, the I_D-V_G characteristics are calculated by the simulator. Then, each method is applied to these I_D-V_G characteristics, and N_t is derived (denoted $N_{t_{out}}$). If a derived $N_{t_{out}}$ coincides with the $N_{t_{in}}$, the method is found to give true N_t.

Our device simulator has two other parameters; the mobility in the grain (μ_0) and increment of band gap at grain boundary (V_{Ba})[4] as shown in Fig.2. These are independent of N_t.

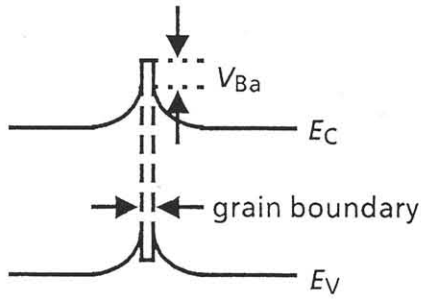

Fig.2. Schematic band diagram near grain boundary assumed in device simulator.
If amorphous region exists near grain boundary, band gap increases by V_{Ba}.

In Fig.3, $N_{t_{out}}$ is shown for various μ_0's and V_{Ba}'s with fixed $N_{t_{in}}$. It is found that the estimated N_t by Levinson's method changes depending on μ_0 and V_{Ba}. On the other hand, the N_t by our method always coincides with $N_{t_{in}}$ with good accuracy. From these facts, we conclude that our method represents an improvement over the ability of Levinson's method to accurately estimate N_t.

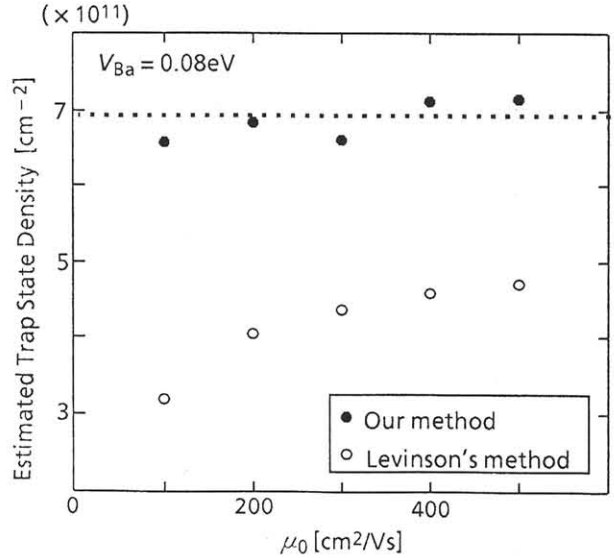

Fig.3 (a). Estimated N_t for calculated I-V characteristics with various μ_0.
N_t used in simulation is 6.94×10^{11} cm^{-2} (indicated by doted line).
t_{ch} used in Levinson's method is 400Å.

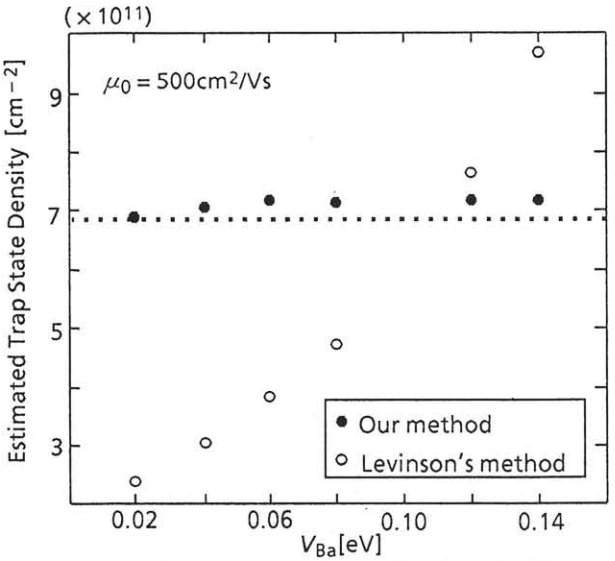

Fig.3(b). Estimated N_t for calculated I-V characteristics with various V_{Ba}.

5. Application to Actual Devices

When our method is applied to actual devices, the flat-band voltage V_{FB} is necessary to calculate n_0. The V_{FB} is determined by charge pumping method[5]. After that $(\partial I_D/\partial V_G)$ - $1/n_0$ relation is plotted as Fig.4. The gate voltage ranges from $(V_{FB}+2)$V to $(V_{FB}+3)$ V. Because of the linearity of this plot, our method is considered to be applicable for this device. From the gradient of the slope, $N_t = 9.09\times10^{11}\mathrm{cm}^{-2}$ is derived.

Using our method, the relation between TFT performance and trap state density is investigated for laser crystallized poly-Si TFTs. The results shown in Fig.5, presents good correlation.

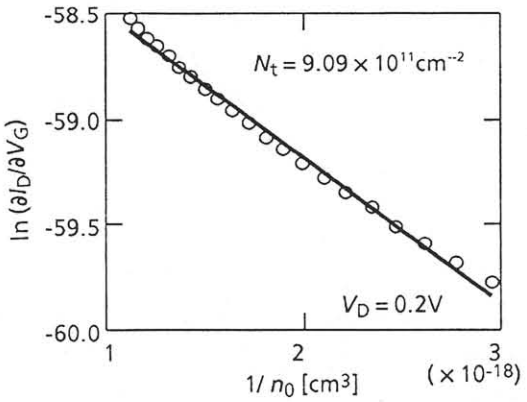

Fig.4. $\ln(\partial I_D/\partial V_G)$ vs $1/n_0$ plot. V_{FB} is -0.8V.

6. Conclusion

We proposed a new method of calculating the grain boundary trap state density by modifying Levinson's method, in which only surface current was considered. The validity of the assumption in our method was confirmed by device simulation. If the conduction model of poly-Si TFT is correct, our method can give the true N_t. Since it is free from the indefinite parameter t_{ch} used in the Levinson's method and is valid for low gate voltage, it is superior to the Levinson's method in quantitative accuracy.

References

1) J.Levinson et al.: J. Appl. Phys. **53** (1982) 1193.
2) R. E. Proano et al.: IEEE Trans. Electron Devices **ED-36** (1989) 1915
3) S. Yamada, et.al.: *Extended Abstracts of the 22nd Conf. SSDM, 1990* 1003
4) N.C.Lu et.al.: IEEE Trans. Electron Devices **ED-30** (1983) 137
5) M. Koyanagi et.al.: *IEDM Tech.Dig. 1990* 863

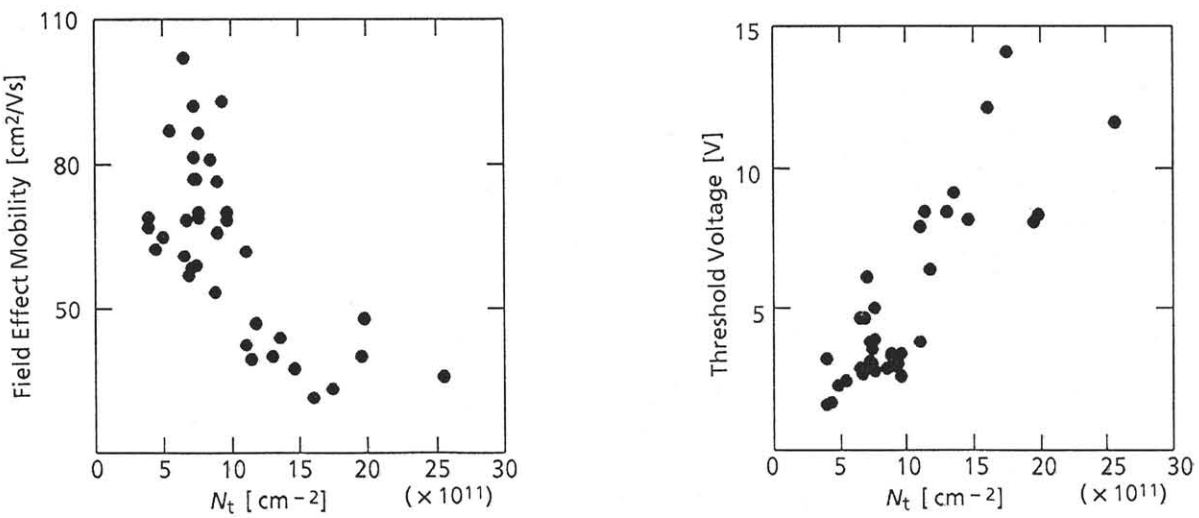

Fig.5. Relation between TFT performance and trap state density.