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Threshold Voltage Shift of a-Si TFTs during Pulse Operation

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The threshold voltage shift of amorphous-Si TFT's under pulse operation is discussed. The duty ratio and frequency dependence of the shift have been measured. A positive pulse stress causes a shift equivalent to that of DC voltage stress. On the other hand, a negative pulse stress decreases the amount of the shift depending on its pulse width and can be accurately described by an equivalent circuit model. Based on these data, a more dependable estimate of the long-term reliability of an amorphous-Si TFT panel has been realized.

1. Introduction

Amorphous-Si (a-Si) TFTs have been widely used in active-matrix LCDs because of their good switching characteristics. However, the threshold voltage (Vt) shift during operation still shows an obstinate instability of a-Si TFTs. Much effort has been done to reduce the amount of the Vt shift, (1) to study the shift mechanisms, (2) and to estimate the long-term reliability by their dependence on the stress period and voltage. (1) It is important to confirm the estimation methods and to verify the panel life-time, because the shift direction is subject to stress polarity, and the resultant shift will be negligible by offsetting shifts of mutually oposite directions. Nevertheless, the investigation has mainly concentrated on applying DC voltage on the gate electrode, and the shift under pulse operation has not been studied in detail. In this paper, the Vt shift under pulse operation is described, and the estimate of the threshold voltage shift of such TFTs under long-term operation is presented.

2. Experiments

As shown in Fig. 1, TFTs used to study the shift have an inverted stagger structure with a gate insulator layer and an a-Si layer between the gate and the source and drain electrodes. The gate insulator layer is composed of silicon-nitride and aluminum-oxide, described in detail elsewhere. (3)

The threshold voltage is defined as the gate voltage at the intersection of extrapolation of the $\sqrt{Id}$ vs. Vg curve in the saturation region. The Vt shift is derived by measuring the Vt before and after applying the stress voltage. In the pulse stress measurements, a rectangular pulse is applied to the gate electrode with the source-drain electrodes set at 0 V. The total stress time is constant in every experiment.

3. Results and Discussion

3.1 Vt shift by pulse stress

Figure 2 shows the duty ratio dependence of the ΔVt with 60 Hz pulses at 25℃. With a positive stress, the positive shift is almost constant with respect to the duty ratio. There is no difference between the shift by pulse stress (○ plots) and that by DC voltage stress (● plots). A negative stress also shows no clear variation with the duty ratio, but there is a sharp jump between the pulse and DC stresses. The DC stress causes a shift to the negative direction (▲ plots) about three times greater than the pulse stress (△ plots).

Figure 3 shows the frequency dependence of the shift with a negative pulse stress having a 50% duty ratio, at 25℃ (○ plots) and 60℃ (● plots). The shift towards the negative direction is greater at 60℃ than at 25℃. A high-frequency pulse decreases the shift. The shift starts to decrease at around 1 Hz at 25℃ and 10Hz at 60℃. In LCD panel operation, a negative pulse is applied at 60 Hz, which causes about a 70% drop in the shift at 25℃ and about a 20% drop at 60℃.

3.2 Effects of pulse stress

Since the threshold voltage shows a negative shift with a negative stress, the shift should mainly be caused by carrier trapping at a-Si / SiN interface. Therefore, when TFTs are stressed by pulse voltage, the

voltage across the gate insulator (Vi) should be taken into account. Vi is calculated through the ordinary charging model of CR circuits, as shown in Fig. 1.

$$Vi = Vg\left(1-\frac{Ci}{Cs+Ci}\exp\left(-\frac{t}{\tau}\right)\right) \quad , \qquad (1)$$

$$\tau = (Cs+Ci)\cdot\left(\frac{1}{Rs}+\frac{1}{Ri}\right)^{-1} \quad , \qquad (2)$$

where Vg is the applied voltage to the gate electrode, Ci and Cs are the capacitances, Ri and Rs are the resistances, of the insulator film and the a-Si film, respectively, t is the stress time, τ is the time constant of the circuit.

When the negative pulse at 60Hz is applied to the gate at 25℃, the ratio of Vi to Vg is calculated as a function of pulse width using expression (1), where the specific resistivity of a-Si is assumed to be 4×10^{10} Ωcm at 25℃ and the a-Si film thickness is 0.24 μm. The ratio varies with the duty ratio, in other words, the pulse width. When the duty ratio is 99.9%, the gate insulator is stressed by 74 % of the applied voltage.

Since the shift is proportional to the stress voltage to the power of 3.8, according to our measurements, we can calculate the amount of the Vt shift by pulse stress from the observed shift by DC stress. The result of this calculation is shown as solid line in Fig 2. In particular, there is a jump in the curve between 99.9% and 100% (DC stress), and the shift with the pulse stress is expected to be 34% of the shift with the DC stress.

On the other hand, when a positive pulse is applied to the gate, the gate insulator is stressed by almost a full-swing voltage, because the a-Si film resistence (Rs) becomes sufficiently low and the time constant (τ) of expression (2) is close to zero, and the voltage across the gate insulator (Vi) is nearly equal to the applied voltage (Vi). Thus, the positive pulse stress causes a shift equivalent to that with DC voltage stress, as shown in Fig.2.

Furthermore, the frequency dependence of the shift can be calculated in the same way, where the specific resistivity of a-Si at 60℃ is assumed to be 2×10^{9} Ωcm. Since the specific resistivity increases at 60℃, the time constant τ becomes small, according to expression (2). Therefore, the shift at 60℃ begins to decrease at higher frequency than that at 25℃. The result is shown in Fig 3 as a solid line and agrees with the data. Thus, the shift with the pulse stress can be explained by the charging model described above.

3.3 Estimate of Vt shift during LCD operation

The basic procedure for estimating the threshold voltage shift during LCD operation is same as reported elsewhere. (1) The shift is obtained as the sum of the ΔVt for a negative and positive bias.

$$\Delta Vt = \Delta Vt(+) + \Delta Vt(-) \quad , \qquad (3)$$

$$\Delta Vt(+) \propto (Vg-Vt)^{\alpha 1}\cdot t^{\beta 1} \quad , \qquad (4)$$

$$\Delta Vt(-) \propto (Vg-Vt)^{\alpha 2}\cdot t^{\beta 2} \quad , \qquad (5)$$

where ΔVt(+) is the shift by positive stress and ΔVt(-) by negative stress. As value $\alpha 1$ and $\alpha 2$ are used 2.7 and 3.8, respectively. The value of $\beta 1$ and $\beta 2$ have been measured at 60 ℃ by DC stress experiment to be 0.54 and 0.47, respectively. We calculated the ΔVt of the LCD panel at 60 ℃, assuming the effective voltage of the negative stress to be 95% of the original voltage. The result is shown as a solid line in Fig. 4 , where a dashed line indicates the result estimated by a conventional method for reference. The estimation of the threshold voltage has been improved to less than 2 V in ten years even at 60℃.

4. Summary

The threshold voltage shift of a-Si TFTs under pulse operation is quite different from that under DC bias. Although a positive stress causes an equivalent shift between pulse and DC stresses, a negative stress causes a sharp jump between 60 Hz pulse and DC stresses. Moreover, the frequency dependence of the shift by a negative pulse stress is remarkable and varies with temperature. These characteristics are explained well, by considering the effective voltage across the gate insulator. Consequently, when the a-Si TFTs are stressed by a negative bias during LCD operation, the expected negative shift is 34% at 25℃, and 82% at 60℃, with respect to the DC stress. Furthermore, the long-term reliability of a-Si TFTs can be estimated more precisely than before, using the data from DC stress measurements.

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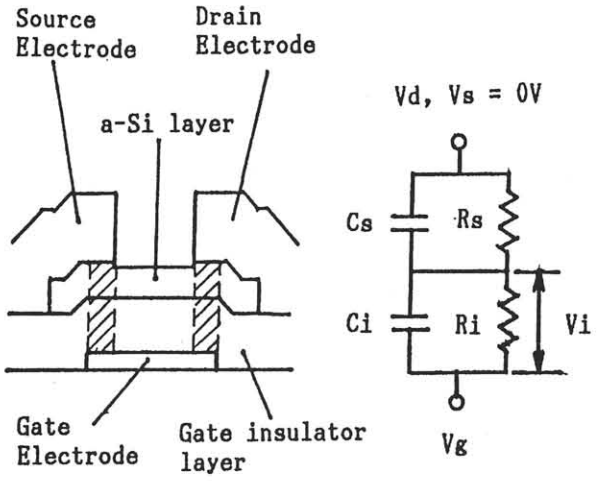

Fig.1 Cross-sectional view of a-Si TFT(left); Equivalent circuit of shaded part(right); Cs and Ci are capacitances of a-Si and gate insulator film, and Rs and Ri are the resistances of a-Si and insulator film, respectively.

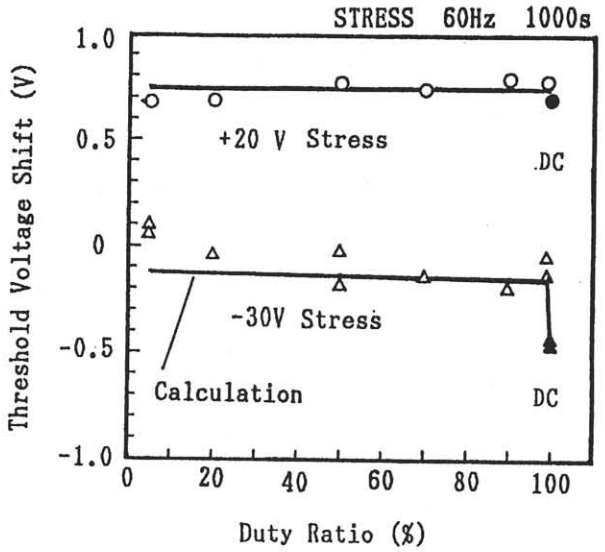

Fig. 2 Duty ratio dependence of shift (ΔV_T) with positive stress (O) and negative stress (Δ)

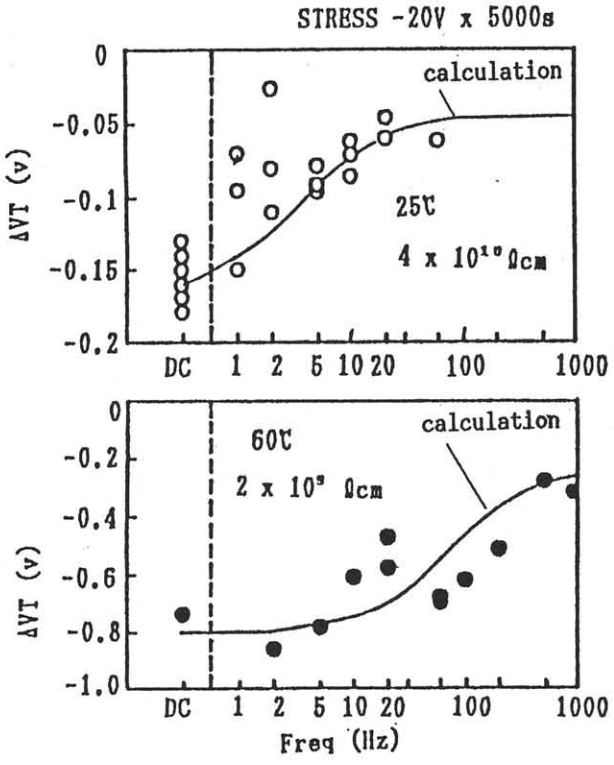

Fig.3 Frequency dependence of shift (ΔV_T) at 25℃ (O) and 60℃ (●)

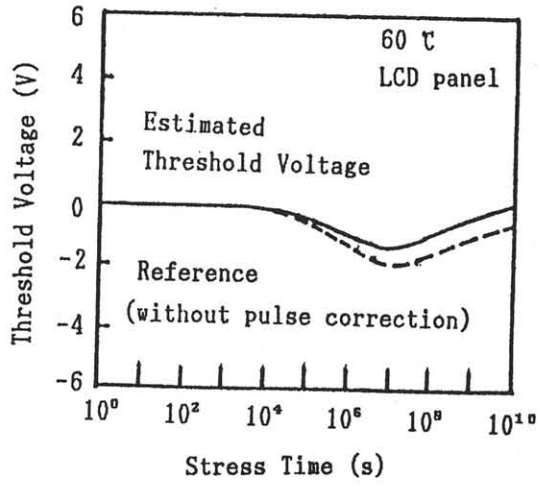

Fig. 4 Estimate curve of the threshold voltage of the LCD panel in panel life time. Dashed line is a conventional result without correction of pulse stress.