

Low Temperature Poly-Si TFTs Using Solid Phase Crystallization (SPC) of Very Thin Films and an ECR-CVD Gate Insulator

Thomas W. LITTLE, Ken-ichi TAKAHARA, Hideki KOIKE, Takashi NAKAZAWA, Ichio YUDASAKA, and Hiroyuki OHSHIMA

SEIKO EPSON CORPORATION
TFT Research Laboratory
Owa 3-3-5, Suwa, Nagano, Japan 392

Low temperature ($T \leq 600^\circ\text{C}$) polycrystalline silicon thin film transistors (poly-Si TFTs) have been fabricated by solid phase crystallization (SPC) of amorphous silicon (a-Si) films deposited by low pressure chemical vapor deposition (LPCVD). These TFTs are distinguished by the very thin nature of the channel Si layer (25 nm) and the use of an SiO_2 gate insulator deposited by electron cyclotron resonance chemical vapor deposition (ECR-CVD). The present process eliminates the need for hydrogenation yet produces mobilities greater than $20\text{ cm}^2/\text{V}\cdot\text{sec}$ and on/off current ratios greater than 10^7 .

1. INTRODUCTION

(Re)crystallization methods such as laser annealing, rapid thermal annealing, and furnace annealing (SPC) have been actively pursued of late as means of producing high quality poly-Si TFTs at low temperatures. Although requiring a sacrifice in processing time, SPC has the potential for a higher degree of both uniformity and reproducibility than the other two processes because of its equilibrium nature. Additionally, SPC is the simplest and least capital intensive of the (re)crystallization methods.

The present paper shows that, contrary to popular practice, the use of very thin films for SPC coupled with an ECR-CVD SiO_2 layer results in TFTs with high mobility and low off current which gives them the potential for use in both driving circuits and pixel transistors in liquid crystal displays (LCDs).

2. TFT FABRICATION

The TFTs used in the present study are fabricated by the following process. Following source and drain formation by *in situ* doped LPCVD poly-Si, a very thin channel layer of 25 nm of a-Si is deposited by LPCVD. The wafer is then annealed in N_2 ambient at 600°C to effect crystallization of the channel Si prior to photoetching. (This crystallization step constitutes the highest processing temperature in the low temperature fabrication process.) The gate insulator is formed by a 2-layer deposition process consisting of an initial layer of SiO_2 deposited by ECR-CVD and a secondary layer of atmospheric pressure CVD (APCVD) SiO_2 . The device is completed by deposition

and patterning of the Cr gate electrode, ITO pixel electrode, and Al source line.

3. EXPERIMENTAL RESULTS

A. SPC of Very Thin Films

The general relation between SPC film thickness and grain size is shown in Fig. 1. Although the exact dependence of grain size on film thickness may change as a function of deposition and annealing conditions^{1,2}, the trend of increased grain size for thicker films generally holds. Therefore, in an effort to minimize the deleterious effects of grain boundaries in poly-Si TFTs, the use of thick films which reduce the grain boundary area for the channel layer may seem warranted. Such an approach may indeed be successful if the ultimate aim is fabrication of TFTs only for driver elements which require high mobility. The concomitant increase in off current with increasing channel film thickness, however, makes TFTs fabricated with thick Si layers unsuitable for pixel TFTs.

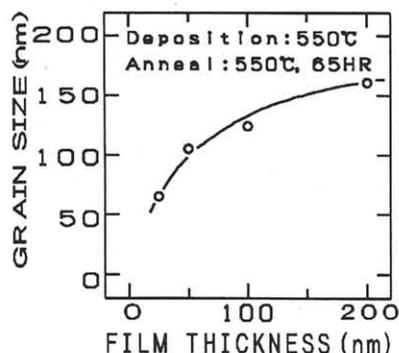


Fig. 1 Poly-Si grain size as a function of film thickness for SPC Si films.

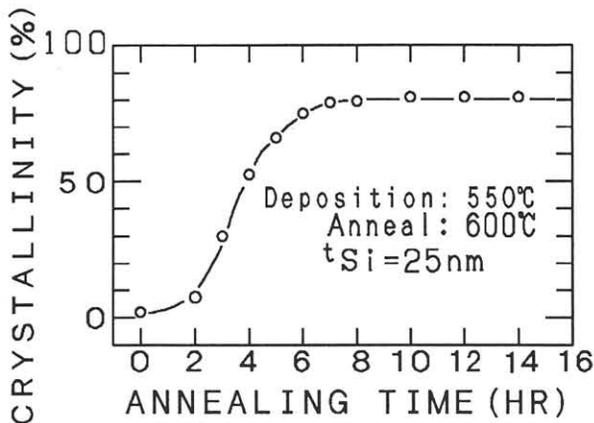


Fig. 2 Crystallinity of 25 nm SPC Si films deposited at 550°C as a function of annealing time at 600°C as measured by ellipsometry.

The use of very thin Si layers in poly-Si TFTs is not new^{2) 3) 4)}. The present study, however, is believed to be the first in which SPC has been used with very thin as-deposited a-Si films in an entirely low temperature process.

Fig. 2 shows crystallinity of 25 nm SPC films measured by spectroscopic ellipsometry as a function of annealing time at 600°C. Fig. 2 reveals that crystallinity saturates after approximately 8 hours. This behavior has been observed repeatedly and confirmed by Raman spectroscopy indicating that SPC is a highly repeatable process. Aside from such reliability and repeatability, the significance of Fig. 2 lies in the relatively short annealing time of 8 hours which not only allows the use of glass substrates but also is amenable to mass-production processing.

Fig. 3 shows a comparison of 25 nm as-deposited and SPC poly-Si TFTs and highlights the improvements offered by SPC.

The benefits of using very thin SPC Si films are clearly shown in Fig. 4. On/off current ratios decrease drastically from a high of greater than 10^7 for very thin films to the order of 10^5 for films of 50 nm or more. This is primarily a consequence of increased off currents caused by the increased conductance of thicker Si layers.

B. ECR-CVD Gate Insulator

In low temperature processed poly-Si TFTs, the importance of the gate insulating layer⁵⁾ takes on even more significance as a consequence of the incompatibility of thermal oxidation. Recent work has shown that high quality SiO₂ layers with properties similar to those of thermal SiO₂ can be deposited by ECR-CVD⁶⁾. The present study confirms the beneficial nature of an ECR-CVD film. Fig. 5 shows the relation between surface state density and the composition of an SiO₂ double layer composed of an initial layer of ECR-CVD followed by a layer of APCVD⁷⁾. The benefits

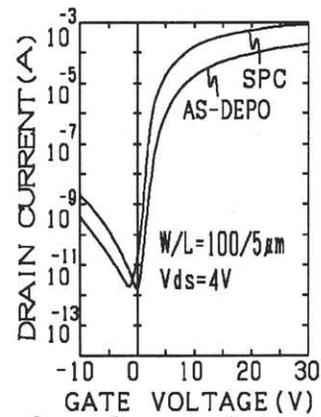


Fig. 3 Transfer characteristics of 25 nm as-deposited and SPC poly-Si TFTs. W/L=100/5 μm.

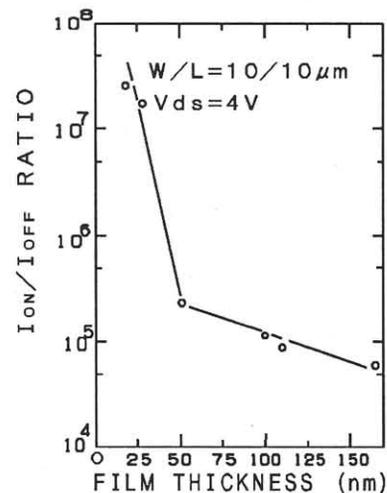


Fig. 4 On/off current ratios of SPC poly-Si TFTs as a function of channel Si film thickness. TFT size: W/L=10/10 μm.

are even more apparent when comparing TFTs fabricated with an APCVD layer to those fabricated with an ECR-CVD/APCVD double layer as shown in Fig. 6. It is not clear at present whether the vast improvement in

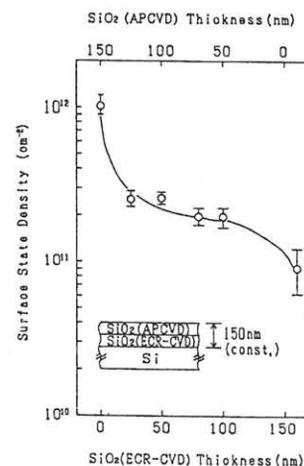


Fig. 5 Relation between surface state density and composition of ECR-CVD/APCVD double layer SiO₂ insulator.

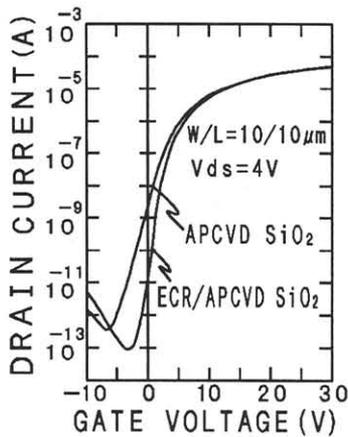


Fig. 6 Transfer characteristics of 25 nm SPC poly-Si TFTs formed with single layer APCVD SiO₂ (150nm) gate insulator and double layer ECR-CVD (50 nm)/APCVD (100 nm) SiO₂ gate insulator. W/L=10/10 μm.

subthreshold slope and minimum current afforded by the ECR-CVD layer is the result of the oxygen plasma cleaning treatment immediately prior to SiO₂ deposition or the possible incorporation of more hydrogen into the Si film during the ECR deposition.

Most studies involving SPC have relied on the combination of relatively thick films (>50 nm) and subsequent hydrogenation (for example^{8,9}). The use of very thin SPC films and ECR SiO₂, however, eliminates the need for a separate hydrogenation step. Fig. 7a shows the improvement in TFT characteristics resulting from hydrogenation of a single layer APCVD SiO₂ TFT while Fig. 7b reveals that, other than a slight shift in threshold voltage, there is no change in TFT characteristics after hydrogenation for an SiO₂ double layer. The characteristics of the APCVD+hydrogenation TFT are almost identical to those of the unhydrogenated ECR-CVD/APCVD double layer TFT. The ECR-CVD/APCVD double layer TFT has mobility of ~24 cm²/V·sec and on/off current ratio of more than 10⁷.

4. LCD PANEL FABRICATION

The applicability of the present process has been demonstrated by the fabrication of LCDs using large area substrates. The coupling of SPC of a 25 nm Si film and an ECR-CVD SiO₂ gate insulator layer produces high performance poly-Si TFTs with excellent uniformity over the entire substrate area and results in a vivid color LCD. Details of the LCD panel will be presented elsewhere.

5. CONCLUSION

High performance poly-Si TFTs have been fabricated by an entirely low temperature process using a unique combination of solid phase crystallization of very thin Si films (25 nm) and an ECR-CVD SiO₂ gate insulator. Even

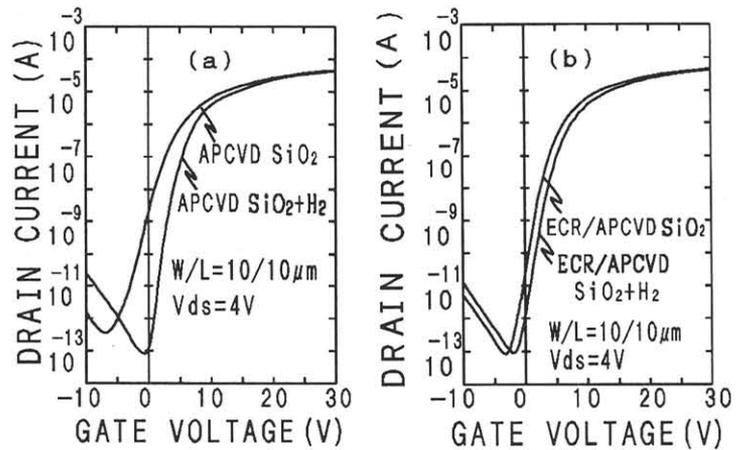


Fig. 7 Effect of hydrogenation treatment on transfer characteristics of TFTs formed with (a) single layer APCVD SiO₂ (150nm) gate insulator and (b) double layer ECR-CVD (50 nm)/APCVD (100 nm) SiO₂ gate insulator. W/L=10/10 μm.

without a subsequent hydrogenation treatment, mobilities greater than 20 cm²/V·sec and on/off current ratios greater than 10⁷ have been achieved. The present process has been successfully applied to fabrication of color LCDs over large area substrates and holds the potential for forming integrated driver and pixel TFTs on the same substrate in the future.

6. ACKNOWLEDGEMENTS

The authors gratefully acknowledge Mr. W. Miyazawa and the pilot line fabrication team for TFT fabrication; the Analysis Center for analytical services; Mr. M. Yazaki, Mr. T. Inami, Mr. S. Inoue, Mr. S. Takenaka, and Ms. R. Takenaka for valuable discussions during the course of this work; and Ms. M. Hirasawa for help in preparing the manuscript.

7. REFERENCES

- 1) M. K. Hatalis and D. W. Greve, *J. Appl. Phys.* **63** (7), 2260 (1988).
- 2) S. Morozumi et al., *Proceedings of the 6th International Display Research Conference*, 196 (1986).
- 3) T. Noguchi et al., *Jpn. J. Appl. Phys.* **25** (2), L121 (1986).
- 4) I. Yudasaka and H. Ohshima in *Polysilicon Thin Films and Interfaces*, MRS Symposium Proceedings Vol. 182, 333 (1990).
- 5) M. K. Hatalis et al., *ibid.*, 357.
- 6) H. Izawa et al., *Extended Abstracts of the 22nd Conference on Solid State Devices and Materials*, 183 (1990).
- 7) H. Ohshima and S. Morozumi, 1989 International Electron Devices Meeting Technical Digest, 157 (1989).
- 8) A. Mimura et al., *IEEE Trans. ED* **36** (2), 351 (1989).
- 9) K. Nakazawa, *J. Appl. Phys.* **69** (3), 1703 (1991).