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Design Considerations for Noncrossing TFT Matrix with Reduced DC Level Shift

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The compensating characteristics for reducing DC level shift in the noncrossing architecture were investigated by using a TFT equivalent circuit model that takes the voltage-dependent TFT gate capacitance into account. Good agreement was obtained between calculated and measured values concerned with the relationship of DC level shift to compensating pulse voltage.

Introduction

TFT matrixes without bus line crossover have been proposed to increase liquid crystal display production yields.[1) 2) 3)] In these architectures, the TFT plate contains parallel scan and reference bus lines, and the counterplate contains the data bus lines so that no bus lines cross. However, this makes storage capacitors difficult to form, and DC level shifts at the pixel electrodes cause image sticking or flicker. Thus, reducing DC level shift is one of the most important obstacles facing practical noncrossing architectures. We propose a new TFT matrix architecture and drive scheme featuring a compensating TFT in addition to the conventional addressing TFT (TFT C and TFT A, respectively, in Fig. 1)[4)] . DC level shift is cancelled by applying a compensating pulse to TFT C. Estimating the proper value of the compensating pulse voltage is important to cancel the DC level shift completely. We therefore analyzed the compensating characteristics, especially the relation between the compensation pulse voltage and the DC level shift.

The compensating action

Figure 2 shows the equivalent cell circuit of our new architecture. V_{GA} and V_{GC} represent addressing and compensating scan pulses. C_{GS}^{A} , C_{GS}^{C} , and C_{LC} are the gate-source capacitances of TFT A, TFT C, and a liquid crystal cell capacitance respectively. V_D represents the data voltage.

Figure 3 shows the timing relationship of scan pulses V_{GA} and V_{GC} , and the pixel electrode voltage, V_S .

During period T1, TFT A is on, TFT C is off and the pixel electrode is connected to the reference voltage by TFT A, so V_S is at zero volts.

During T2, V_S shifts to voltage level V1 due to the capacitance coupling of C_{GS}^{A} just at the time the addressing pulse falls.

During T3, V_S shifts from V1 to V2 due to the capacitance coupling of C_{GS}^{C} just at the time the compensating pulse rises. For successful cancelation, V2 must be close to zero volts. V2 is determined by addressing and compensating pulse voltages and the values of C_{GS}^{A} and C_{GS}^{C} .

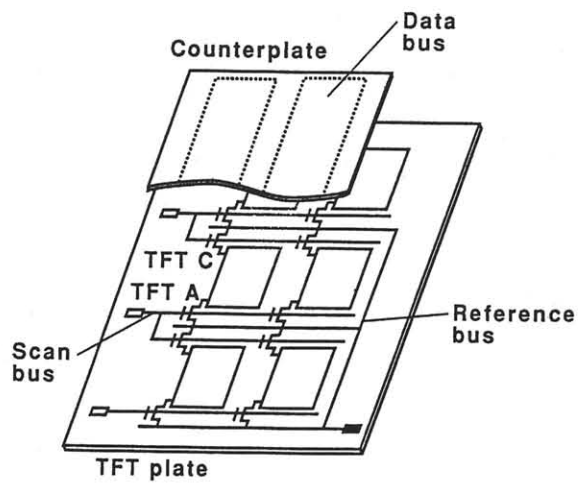

Figure 1 Equivalent circuit of proposed TFT matrix

Voltage dependences of the TFT gate-capacitance

The TFT gate-source capacitances which dominate the DC level shift vary with gate bias conditions. This variance is expressed by the step change model[5] of C_{GS} (on) and C_{GS} (off), the values of C_{GS} with the TFT in the on and off states(Fig. 5). However, the threshold gate voltage, V_{TH}, at which C_{GS} changes cannot be obtained explicitly from the TFT characteristics. Therefore, we analyzed this relationship quantitatively by using an equivalent circuit model of the TFT.

Figure 4 shows the proposed variable gate-capacitance model of the TFT, where C_1, C_2, C_3 and R represent the overlap capacitance between TFT gate and source, the channel capacitance, the overlap capacitance between gate and drain, and the channel resistance. With both the source and drain electrodes grounded, the equivalent gate capacitance in Fig. 4 is expressed as

$$C = C_1 + C_3 + C_2/(\omega^2 C_2^2 (R/4)^2 + 1), \quad (1)$$

where ω represents the measurement angular frequency.

Figure 5 plots the calculated and measured values of gate capacitance with gate voltage. R in Equation (1) was deduced from the measured V_D - I_D characteristics of the TFT. The calculations agree well with the measurements. As Fig. 5 shows, the gate capacitance roughly doubles over the range of gate voltage and remains constant at sufficiently low or high gate voltages.

A detailed analysis of the compensation characteristic

We next used the variable gate-capacitance model to analyze the DC level shift compensation mechanism.

During period T2 in Figure 3, each pulse and capacitance is expressed by the law of charge preservation as

$$\int_{V_{OFF}-V_1}^{V_{ON}} C_{GS}^{A}\, dV_G + C_{GS}^{C}\, V1 + C_{LC}\, V1 = 0 . \quad (2)$$

The gate capacitance of TFT C can be treated as a constant because its gate bias is sufficiently low. C_{LC} is also treated as a constant during level shifting because V1 is small. Equation (1) is useful for gate-source capacitances, C_{GS}^{A} and C_{GS}^{C} in the Equation (2). However, because Equation (1) represents the composite value

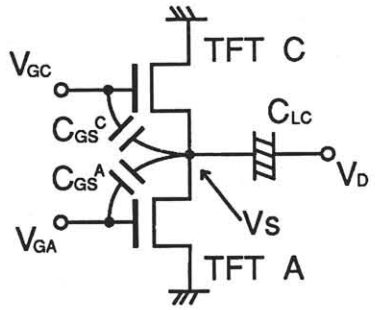

Figure 2 Equivalent cell circuit

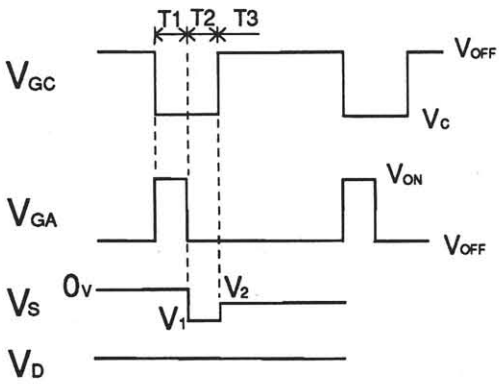

Figure 3 Pulse waveforms applied to cell circuit

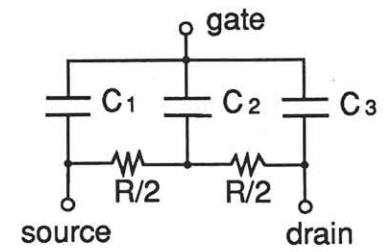

Figure 4 Proposed variable gate capacitance model of TFT

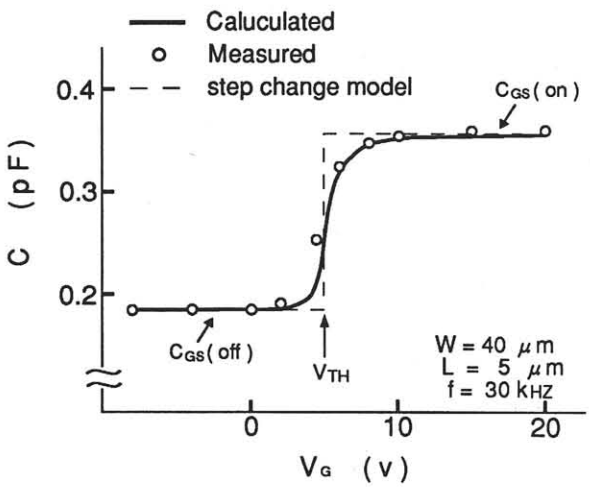

Figure 5 Relationship between gate voltage and gate capacitance

of the gate-source and gate-drain capacitances, we divided the value obtained from Equation (1) by 2 to solve the Equation (2).

During period T3, Equation can be expressed as follows:

$$C_{GS}^{C}\,(V_C - V1 - V_{OFF} + V2) + (C_{GS}^{A} + C_{LC})(V2 - V1) = 0 \quad (3)$$

Figure 6 shows the measured and calculated relationship between the compensating pulse magnitude, $V_{OFF} - V_C$ and the DC level shift, V2, for three compensating TFTs of different dimensions (Table 1). The calculations involved Equations (1) to (3). As shown in Figure 6, calculations and measurements show good agreement, and both have an optimum value of compensating voltage at which level shift voltage V2 becomes zero, independent of the data voltage. This means, in our architecture, that an optimum compensating voltage cancels the DC level shift even though the liquid crystal has capacitance anisotropy.

Figure 7 shows estimations of the compensation for the DC level shift in the conventional architecture, based on the above variable gate-capacitance model comparing with the former results from the noncrossing architecture. In the conventional architecture, different compensating voltages are required corresponding to data differences or data polarities(positive or negative) for cancelling the DC level shift. Therefore the driving scheme will be more complicated than with the noncrossing architecture.

Conclusion

The DC level shift compensating characteristics in a noncrossing TFT matrix architecture was investigated considering the voltage-dependent characteristics of the gate capacitance when the TFT goes off state from on state. Good agreement between calculated and measured values was obtained by adopting the TFT variable gate-capacitance model.

References

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2) J. F. Clerc et al., Digest of Japan Display '86, p.84, 1986
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TFT C dimension (μm)

sample	W	L	GS	GD
A	40	10	10	5
B	20	15	10	5
C	40	5	5	5

TFT A dimension (μm)

sample	W	L	GS	GD
A	20	5	5	5
B	↓	↓	↓	↓
C	↓	↓	↓	↓

GS : gate-source overlap
GD : gate-drain overlap

Table 1 Dimensions of TFT in Fig. 6

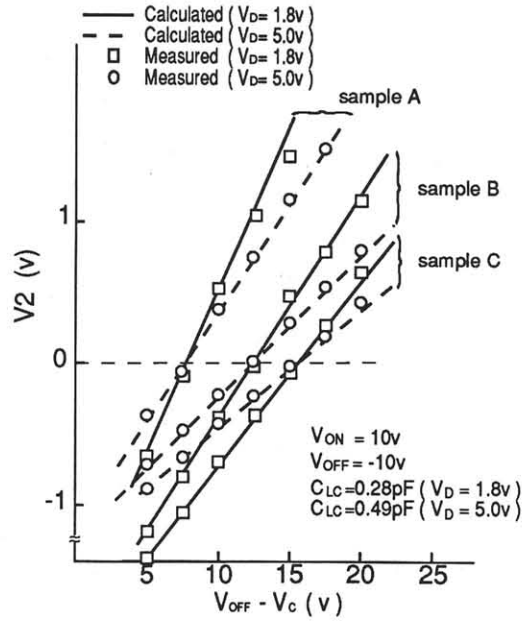

Figure 6 Compensating characteristics - compensating pulse voltage versus DC level shift, V2 for three TFTs

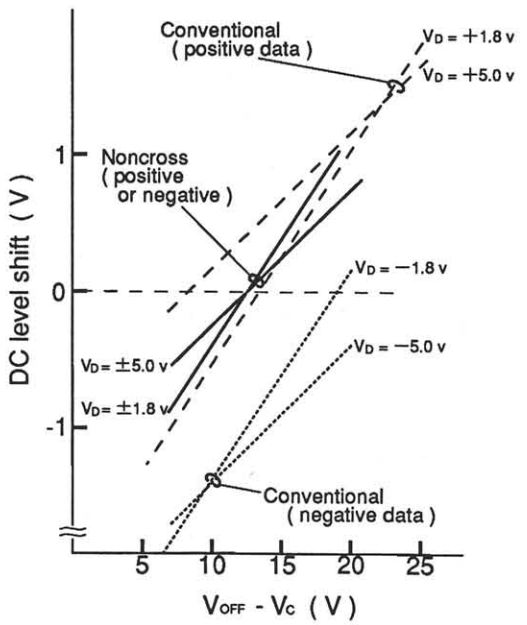

Figure 7 Compensating characterstics for noncrossing and conventional architectures