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Batch-Process for High Performance Amorphous-Silicon Thin-Film Transistors Using Hot-Wall Chemical-Vapor-Deposition Method

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Hot-wall-type low-temperature CVD method has been investigated aiming at batch process for amorphous-silicon thin-film transistors (a-Si TFTs). High performance TFTs (mobility =1.7cm^2/Vs, threshold voltage =9V, and subthreshold voltage-swing =0.8V/decade) have been fabricated with good reproducibility and uniformity.

1. Introduction

Low yield and low throughput are the most serious remaining problems in mass-production of amorphous-silicon thin-film transistor (a-Si TFT) matrices. These problems are caused by inherent properties of the plasma-CVD method, such as (1) generation of dense flakes in the chamber due to plasma-polymerization et al., and (2) difficulty in batch process for depositing the active films simultaneously on many substrates due to plasma potential. Thus, they can be solved only by using an alternative method which does not use plasma.

Recently, we have reported high performance a-Si TFTs produced by low-temperature CVD method using higher silanes[1-2] such as Si_2H_6 or Si_3H_8. The highest field-effect mobilities were 2.2cm^2/Vs for electrons and 0.1cm^2/Vs for holes, respectively. In these studies, we had used the cold-wall CVD system, and the samples were heated by a ceramic heater placed at the center of the chamber. Based on these results, we have developed batch process using a hot-wall reactor. High performance TFTs have been successfully produced.

2. Experimental

A hot-wall type CVD system used in this work is shown in Fig.1. Di-silane (Si_2H_6) gas with (or without) hydrogen gas was introduced from the top of a quartz tube with 3.6cm in diameter, and evacuated by a pump. A batch of samples was placed near the center of the tube (in the flat temperature region of about 15cm long), and heated by an external resistive heater through the tube wall.

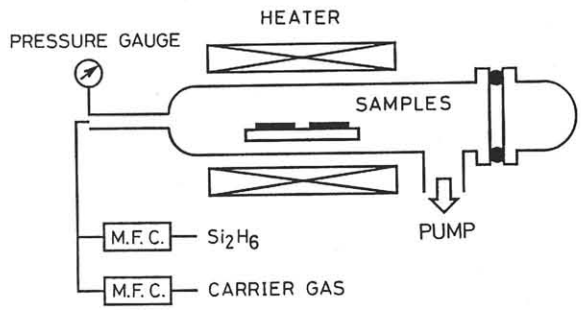


Fig.1 Schematics of hot-wall CVD system.

Table 1 Process flow of TFTs

1) Thermal oxidation	Dry O_2, 1000°C
2) Pre-annealing	H_2: 50sccm, 500Torr
3) a-Si deposition	Si_2H_6: 2.5sccm, H_2: 0-5sccm 1.0Torr, 440-550°C
4) Post-annealing	H_2: 50sccm, 500Torr, 250°C
5) Al evaporation and patterning	
6) HRA	H_2: 30sccm, H_2(Hg): 3sccm, 40Torr, 225°C

Table 1 shows the process flow for the inverted staggered TFT structure. The TFT characteristics were investigated in the deposition temperature range from 440°C to 540°C. Flow rate of Si_2H_6 and pressure were kept constant at 2.5sccm and 1.0Torr, respectively. Thickness of the deposited a-Si film was 35nm±5nm for all samples. After the deposition, the samples were annealed in the H_2 ambient at pressure of 500Torr without breaking the vacuum. Aluminum was then deposited and patterned to form the ambipolar TFT structure. After delineating the active a-Si island, the samples were post-hydrogenated in the photo-generated hydrogen-radical ambient[3].

The channel length and width were 100μm and 200μm, respectively.

3. Results and Discussion

Deposition rate is shown in Fig.2 as a function of reciprocal wall temperature. The rate was as high as 7nm/min at 500°C. The a-Si film had uniform thickness since it was deposited under surface reaction-limited conditions with an activation energy of 2.4eV.

Figure 3 shows the logarithmic drain current I_D, as a function of the gate voltage V_G, at a drain voltage V_{DS} of 10V. Broken curves represent the results before hydrogen radical annealing (HRA). The characteristics were drastically improved by HRA as shown by continuous curves in the figure. This reason could be clearly explained by the fact shown in Fig.4 that hydrogen content in the a-Si layer evaluated by SIMS was increased drastically after HRA. Hydrogen atoms introduced by HRA will effectively terminate dangling bonds which generate deep trap states in the a-Si bandgap.

Due to the absence of blocking contacts, the TFT could be operated in both n-channel and p-channel modes by changing the gate voltage polarity. The typical on/off current ratio was as high as 10^6 at V_{DS}=10V.

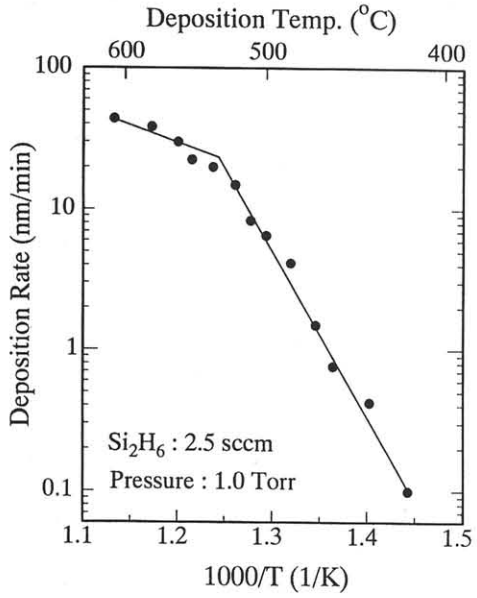


Fig.2 Deposition rate as a function of wall temperature.

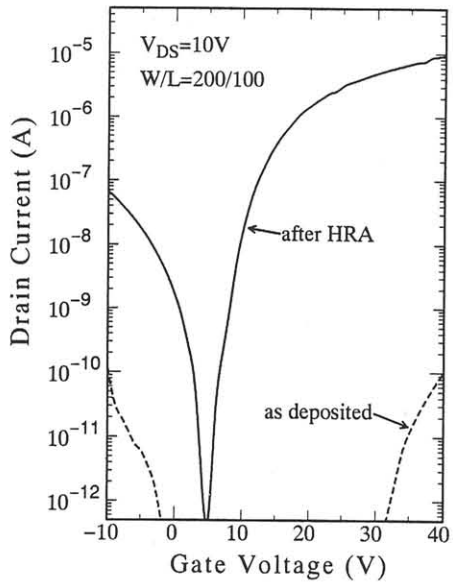


Fig.3 Logarithmic drain-current versus gate voltage for TFTs before HRA (broken curve) and after HRA (continuous curve).

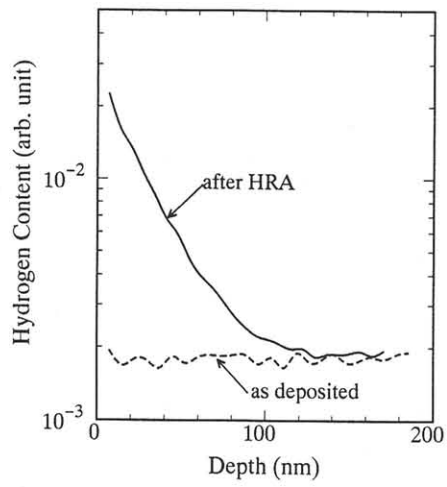


Fig.4 Hydrogen distribution in the a-Si film before and after HRA.

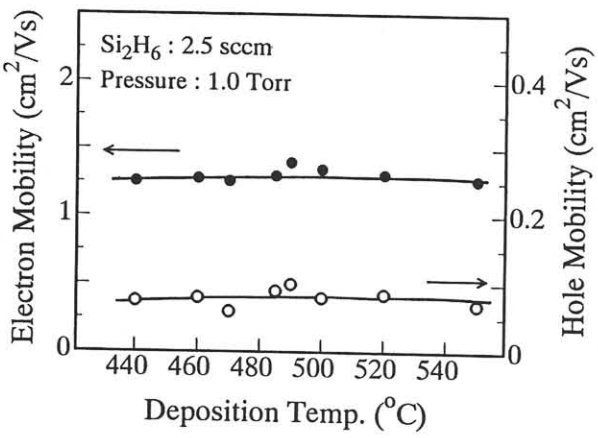
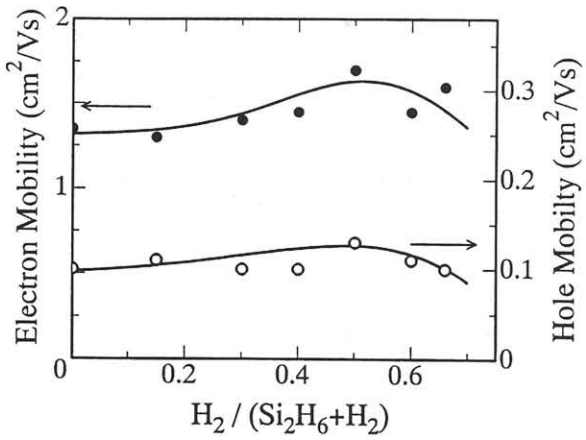
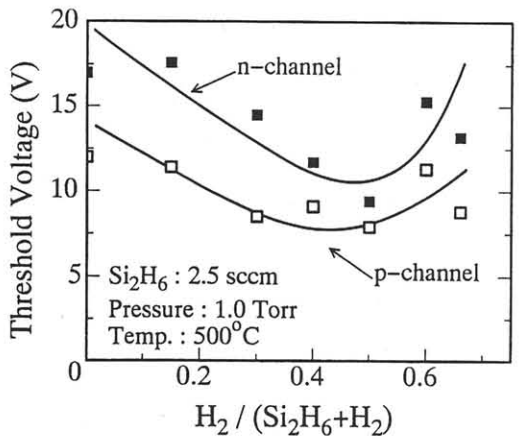


Fig.5 Field-effect mobility as a function of wall temperature.



(a)



(b)

Fig.6 Field-effect mobility (a) and the value of threshold voltage (b) as a function of gas flow rate ratio.

The electron and hole field-effect mobilities are shown in Fig.5 as a function of the wall temperature during the a-Si deposition. The mobilities depend slightly on the wall temperature. It will be worthy to note that the TFT characteristics are the same even for samples in different lots fabricated under the same process condition.

Effects of carrier gas have been investigated, and hydrogen was the most effective. TFT characteristics are shown in Fig.6 as a function of the gas flow rate ratio R (=[H_2]/[H_2]+[Si_2H_6]). The Si_2H_6 flow rate and wall temperature were kept at 2.5sccm and 500°C, respectively. With increasing R, TFT characteristics were improved steadily. For R>0.5, however, the deposition rate was decreased rapidly and thus the TFT characteristics were deteriorated. The best values for the threshold voltage and subthreshold voltage-swing were 9V and 0.8V/decade respectively for the n-channel operation and -8V and 1.2V/decade respectively for the p-channel operation. The highest mobility was 1.6cm^2/Vs for electrons (it was increased to 1.7cm^2/Vs by eliminating parasitic resistance effects), and 0.12cm^2/Vs for holes.

4. Conclusions

We have succeeded in producing a high performance a-Si TFT using hot-wall CVD system. There are important features in this method, namely, (1) high throughput due to batch processing, (2) high yield due to plasma-polymerization-free CVD, and (3) good TFT characteristics with high reproducibility and uniformity. Process temperature can be reduced by tri-silane or tetra-silane.

References

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