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Comparison of Different Processes in the Fabrication of Crystallized Amorphous Silicon Thin Film Transistors

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A comparison of different processes in the fabrication of crystallized amorphous silicon thin film transistors(TFT's) is presented.These processes are : low pressure chemical vapor deposition, plasma-enhanced chemical vapor deposition, furnace annealing, rapid thermal annealing, RF plasma and ECR plasma hydrogenation. Results indicate that high quality TFT's with a leakage current of 10^{-13}A and an on/off current ratio of 10^{9} can be achieved in any combination of these above processes.

In this report, we will make a systematic comparison of different processes in the fabrication of crystallized amorphous silicon thin film transistors (TFT's). These processes are : film deposition (low pressure chemical vapor deposition LPCVD vs. plasma-enhanced chemical vapor deposition PECVD), annealing for silicon crystallization (furnace annealing vs.rapid thermal annealing or RTA)and plasma hydrogenation (RF vs. electron cyclotron resonance or ECR).

LPCVD amorphous silicon films were prepared at 560C with silane at a pressure of 89 mTorr. and a flow rate of 29 sccm, whereas PECVD films were made at 300C from a mixture of silane and hydrogen, 1 Torr.,at a frequency of 13.56 MHz. The furnace annealing was done in a nitrogen atmosphere at 620C for 15 hours, whereas the rapid thermal annealing was at 700C for 4 mins. As for the plasma hydrogenation, RF hydrogenation was carried out at 300C in a mixture of nitrogen and hydrogen, whereas ECR hydrogenation was in pure hydrogen, 600W, at a pressure of 1.4x 10^{-4} [1].Thickness of silicon films used in this study was 1,500A. All silicon films were characterized, using transmission electron microscopy (TEM) ,electron diffraction, scanning tunneling microscopy (STM) to study the grain size, morphology and surface smoothness of the films.

Fig.1 shows photographs of TEM and electron diffraction patterns of crystallized PECVD film with RTA (a), furnace annealing (b) and crystallized LPCVD film with furnace annealing(c) . The average grain size of the annealed silicon films fabricated from different deposition techniques and annealed at different conditions was in the range of 1,500 to 3,000A. Shown in Fig. 2 is the surface roughness of as-deposited PECVD amorphous silicon film (a) and as-deposited LPCVD amorphous silicon film (b). From this Fig. , it was found that roughness of PECVD film is in the range of 8-10A, whereas roughness of as-deposited LPCVD film is about 30-40A. Similarly, crystallized LPCVD film shows a rougher surface (80-100A) than crystallized PECVD film (40-60A).

In order to evaluate the quality of crystallized amorphous silicon films prepared with different processes, thin film transistors were fabricated. The experiment can be explained as follows : First, one micron of silicon oxide was grown for insulation on three-inch silicon wafers. Next, amorphous silicon film (1,500A) was deposited. The wafers were annealed to form crystallized films which were then patterned into islands, using microlithography means. A 1,000A gate oxide was thermally grown at 1,050C in an oxygen atmosphere. After the oxide formation, thickness of the polysilicon channel layer is expected to be

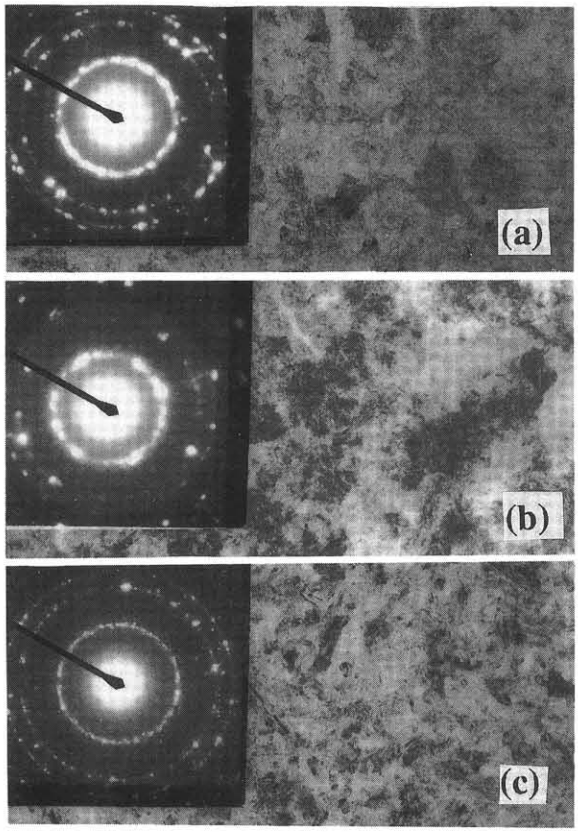


Fig.1 TEM and electron diffraction patterns of crystallized amorphous silicon films : (a) PECVD, RTA, (b) PECVD, furnace annealing and (c) LPCVD, furnace annealing

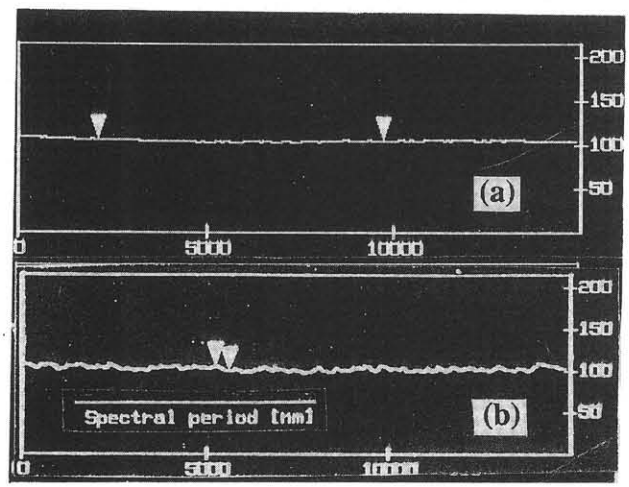
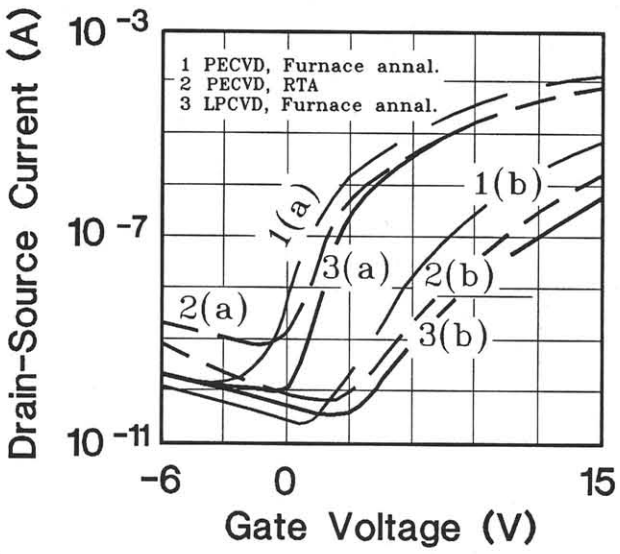


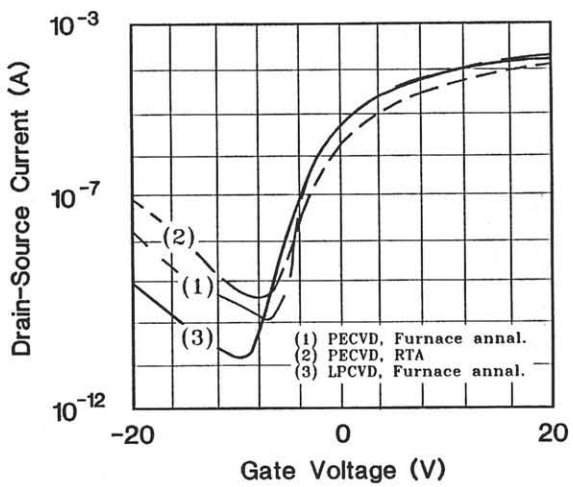
Fig.2 Surface roughness of as-deposited amorphous silicon films: (a) PECVD and (b) LPCVD

about 1,000A. Gate LPCVD polysilicon was then deposited at 620C and patterned. Phosphorus with a dose of $10^{15}/cm^2$ was implanted to dope the source, drain and gate. The dopant was activated during a 30 minute nitrogen annealing at 1,050C. Contact holes were etched through the oxide over the source and drain. Aluminum-silicon alloy was deposited and then annealed at 400C in a mixture of nitrogen and hydrogen for 30 minutes to form a better drain, source and gate contact. Finally, TFT's were hydrogenated by means of either RF plasma or ECR plasma. As shown in Fig. 3(a) for the drain-source current (Ids) vs. gate voltage (Vg) transfer characteristics, before hydrogenation, PECVD films annealed in the furnace gave a better device performance , next was LPCVD films annealed in the furnace, then came PECVD films with RTA. This trend is true for all the devices in different wafers. After RF plasma hydrogenation at a power density of 0.5 W/cm^2 for 2 hours, LPCVD films gave better device performance than PECVD films. TFT's treated in ECR plasma show similar trend and performance, as shown in Fig. 3(b). After being hydrogenated with either RF or ECR plasma, TFT's with a leakage current of 10^{-10} to 10^{-11} and an on/off current of 10^6 to 10^7 were obtained. These results have by no means been optimized yet. From the results shown in Fig. 3, it was found that different hydrogena - tion conditions are required for different sets of crystallized amorphous silicon films to optimize the device performance of TFT's. Ids-Vg transfer characteristics of crystallized amorphous silicon TFT's treated at different optimized conditions for plasma hydrogenation are shown in Fig.4 . All the TFT's show a high quality performance with a leakage current of 10^{-13} A and an on/off current ratio of 10^9.

In conclusion, high quality TFT's can be obtained by any combination of the above processes. However, from the fabrication point of view, it is suggested that a combination of PECVD , RTA and ECR is the process of choice due to the following reasons : (i) large area, high deposition rate, possible integration to PECVD amorphous silicon-based photodiodes for sensor applications(PECVD), (ii) time saving , less contamination (RTA) and (iii) time saving, more reproducibility and less ion bombardment (ECR).



(a)



(b)

Fig.3 Ids-Vg transfer characteristics of crystallized amorphous silicon TFTs. a and b in the bracket stands for after and before hydrogenation, respectively.

(a) RF plasma

(b) ECR plasma

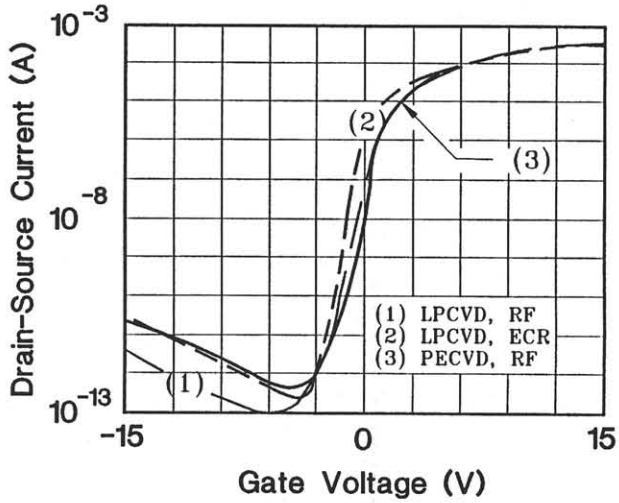


Fig. 4 Ids-Vg transfer characteristics of crystallized amorphous silicon TFT's treated with different optimized conditions for plasma hydrogenation.

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