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Crystallinity Improvement of Small Grained Poly-Si Films by Excimer Laser Annealing for High Performance TFT's

Takashi Noguchi, Hironori Tsukamoto, Toshiharu Suzuki and Haruko Masuya.
Process Technology Div., ULSI R&D Group, Sony Corp.
4-14-1 Asahi-cho, Atsugi-shi, Kanagawa-ken, 243, JAPAN

Excimer laser annealing(ELA) was applied to fabricate poly-Si TFT's with small controlled grain size. Remarkable improvement of characteristics has been observed when the poly-Si surface is smooth and small grain sizes are kept below 800Å. Field effect hole mobilities greater than $35cm^2/V.s.$ and gate voltage swings below 180mV/dec. have been obtained. Moreover, by adapting the offset drain structure, low leakage current as low as $2X10^{-14}A/\mu m$ could be attained. The improvement in characteristics was attributed to an improvement of crystallinity in grains and at grain boundaries.

1. Introduction

Active research on TFT's is being undertaken not only for Liquid Crystal Displays (LCD)[1,2] but also for SRAM's[3]. It is reported that smaller grains compared to the channel length are favorable to make TFT characteristics uniform[4], although carrier mobility decreases. While high temperature annealing can improve these electronic properties of poly-Si films, ELA is considered to be an advanced RTA process[5,6], as it causes no thermal effect to the underlying devices and substrate. We investigated the ELA effect on the improvement of crystallinity and related electronic properties of small grained poly-Si films, and the obtained TFT characteristics were evaluated.

2. Experiments

Si films of 400Å thickness were deposited on SiO_2/Si substrates by LPCVD. Films with small grain sizes were obtained by low doses of Si^+ implantation and subsequent solid phase growth at 600°C as shown in Fig.1[7]. After that, a CVD SiO_2 of 500Å thickness was coated on the poly Si films for anti-contamination and anti-reflection at 308nm. The films were irradiated by a uniformly shaped single pulse from an excimer laser(308nm) varying the energy density below $300mJ/cm^2$. For these films, the crystallinity of the films was analyzed by TEM and UV reflectance spectroscopy. Also, by using these films, p-channel TFT's with a channel geometry of W/L=10/1(μm/μm) and CVD gate oxide of 300Å were fabricated. Source and drain were formed by a 600°C furnace annealing, that is, a low temperature TFT process was employed. In order to reduce the leakage current further, an off-set drain was constructed by oblique ion

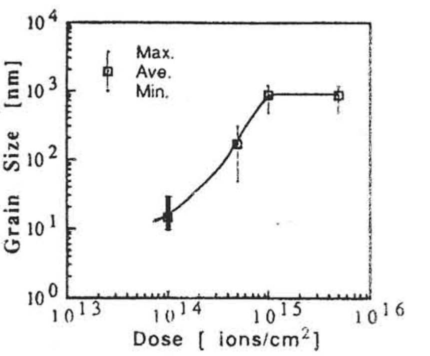


Fig.1 Obtained grain size after SPG(Solid Phase Growth) as a function of Si^+ dose.

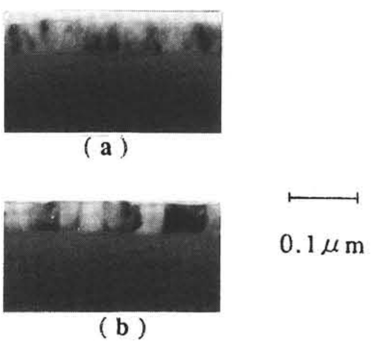
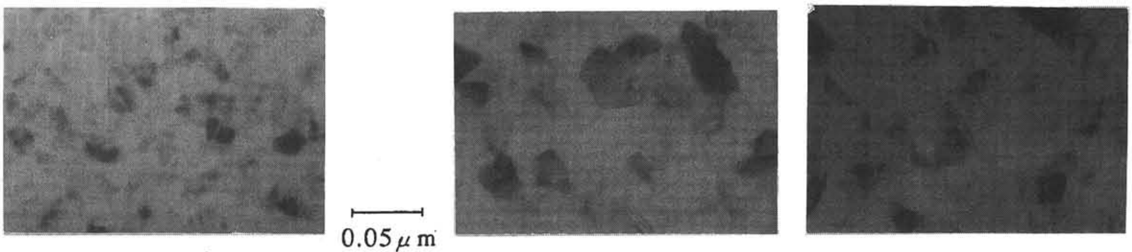


Fig.2. c-TEM images (a) before and (b) after ELA ($219mJ/cm^2$).



(a) 0 mJ/cm^2 (b) 180 mJ/cm^2 (c) 232 mJ/cm^2

Fig.3 TEM images for various pulse energy densities.

implantation of 30° using the gate as a mask. Finally, hydrogen was incorporated by annealing passivated plasma SiN films for terminating the defective silicon bonds. Basic TFT characteristics such as field effect mobility, threshold voltage and leakage current were evaluated.

3. Results and Discussion

For pre-crystallized films with small grains of about 200Å formed using a low Si^+ dose of $1X10^{14}/cm^2$, the grain sizes slightly increase with surface flatness and the sizes stay below 800Å after ELA, as shown in Fig.2, Fig.3 and Fig.4. Image of grain boundaries by TEM analysis changed to be more obvious and the lattice images in grains appeared clearly after ELA above $180mJ/cm^2$. A UV reflectance peak at 4.4eV[7] increased remarkably with increasing ELA pulse energy density as shown in Fig.5. This implies that the crystallinity at grain boundaries and in grains improved effectively after ELA. As the energy density increased to above $200mJ/cm^2$, the field effect hole mobility deduced from TFT characteristics increased to over $35cm^2/V.s.$ and the gate voltage swing decreased to below 180mV/dec.(Fig.6 and Fig.7). It is reported that the melting point of amorphous silicon is fairly lower than that of silicon in the crystalline phase[8]. The marked improvements by ELA below about $250mJ/cm^2$ was speculated to be caused by melting mainly the defective regions in the films. Crystallinity improvement after ELA suggests that trap states density at grain boundaries as well as in grains decreased after ELA. Effective trap states density is related to the gate voltage swing of TFT characteristics as,

$$S=kT/q \cdot \ln 10 \ (1+qdN_t/C_{ox}). \qquad (1)$$

For TFT's with an off-set drain, quite low off-currents below $2X10^{-14}A/\mu m$ have been measured, having high on/off ratios as shown in Fig.8(c). Decreasing the electric field near the drain is effective for reducing the off-current as well as decreasing the trap states density.

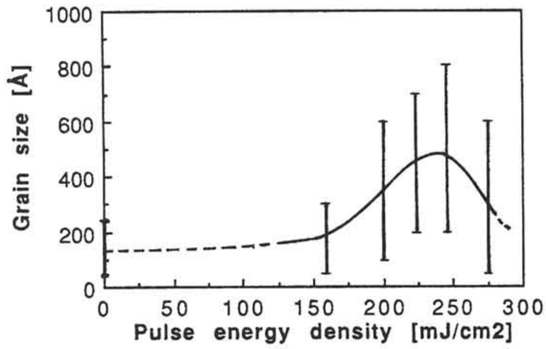


Fig.4. Grain size obtained by TEM images.

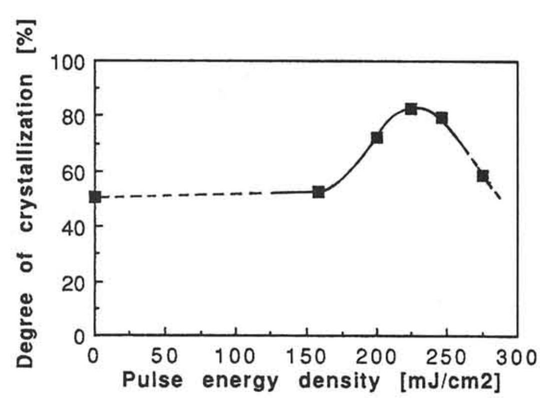


Fig.5. Degree of crystallization deduced from UV reflectance peak spectra[7].

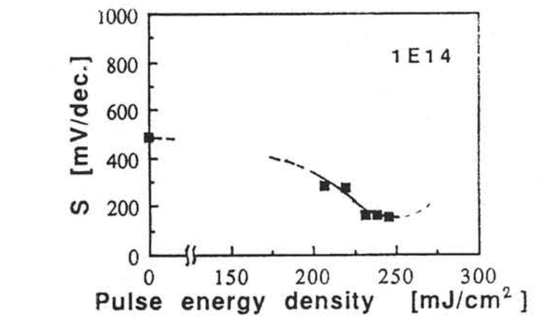


Fig.6.

Field effect mobility vs. pulse energy density.

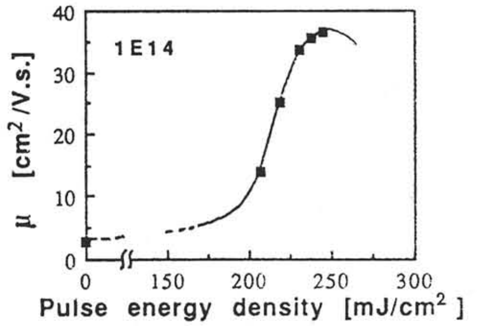
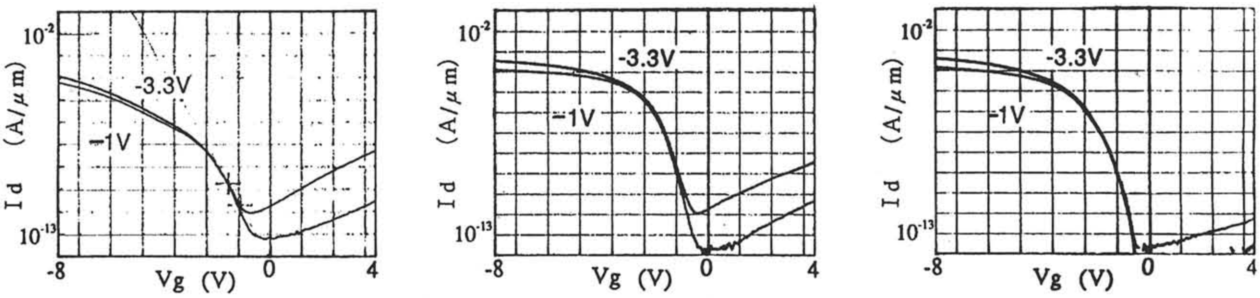


Fig.7.

Gate voltage swing vs. pulse energy density.



(a) 0 mJ/cm^2 (b) 238 mJ/cm^2 (c) 236 mJ/cm^2 (off-set. drain)

Fig.8. Basic TFT characteristics. [W/L=10/1(μ m/μ m), tox=300Å]

These superior characteristics of TFT's with such small grains are expected to have an advantage for forming uniform TFT's in ULSI applications when uniform energy control over the wafer or glass substrate can be attained. Also, ELA can ensure high throughput when we control it by step and repeat methods with a uniform beam pulse like that of a lithographic aligner.

4. Conclusions

By analyzing the crystallinity of the films and evaluating the TFT characteristics, we confirmed that ELA processing improves TFT characteristics remarkably. The surface is kept flat and the grains small. Therefore, small grained poly-Si films with improved crystallinity by ELA can be applied to highly integrated stacked SRAM's and LCD's built on glasses with low melting points.

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