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On The OFF-Characteristics of a-Si TFT With The n/i Buffer Layer

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I. Introduction

Amorphous silicon alloy thin-film transistors(TFTs) have a potential to become a variable and important technology for large-area, low-cost integrated circuits. These circuits are currently being used to drive large-area liquid-crystal displays. Basic integrated circuits(ICs) and addressable image sensing arrays have also been implemented[1][2][3], All of these have focused in so-called "Giant Electronics"[4], which is the opposite of "Micro Electronics".

There are many important factors in a-Si TFTs to affect the quality of display when a-Si TFTs are practically used in display area, which have long been an obstacle to many practical applications of this technology. Of these factors, On-current and Off-Current are the most important quality factors for the TFT used in the large-area liquid-crystal displays, since the former restricts the minimum refresh time of the TFT matrix and the latter restricts the maximum retention time of the matrix.

II. Experimental Outline

There are various origins of the off-current in the a-Si TFTs[5]. Among them, the hole current, i.e., the p-channel operation under the negative V_G conditions, is the most serious in the a-Si TFT. Introduction of an n^+ drain can depress, in principle, the hole current by the effect of its blocking function agaist holes, but its effectiveness is limited in practice, due to dense generation-recombination centers at the n^+-i a-Si interface. In order to obtain good off-characteristics, we have proposed a novel a-Si TFT with a buffer layer at the n^+-i a-Si interface.

A bottom gate invert-staggered a-Si TFT was used in the experiment. After the Cr gate electrode was patterned, a 4000-Å-thick a-SiNx: H gate dielectric and a 2000-Å-thick a-Si: H layer were successively deposited on the gate electrode by RF glow discharge in a PECVD apparatus with separated chambers. A buffer layer of thickness d_B was then deposited by RF glow discharge of the gas mixture of silane(SiH_4) and hydrogen(H_2) in the chamber used to deposite the n^+ layer and the n^+ layer was successively fabricated in the same chamber. Finally, aluminum was patterned to form the drain and source electrode.

The effects of the thickness of the buffer layer on the off-current of a-Si TFT is obvious in our experiment. It was shown that the off-current of a-Si TFT could approach to the magnitude of 10^{-13}A when the thickness d_B of the buffer layer was about 50Å, which is indicated in Figure 1.

III. Theoretical Considerations

As we all known, there is a distance for the electrons to reach the source electrode from the channel under the gate electrode in the case of a bottom gate invert-staggered a-Si TFTs. Thus, the movement of the electrons and holes is affected by the electric field across the i and

n layer. Based on these considerations, we have studied the electric

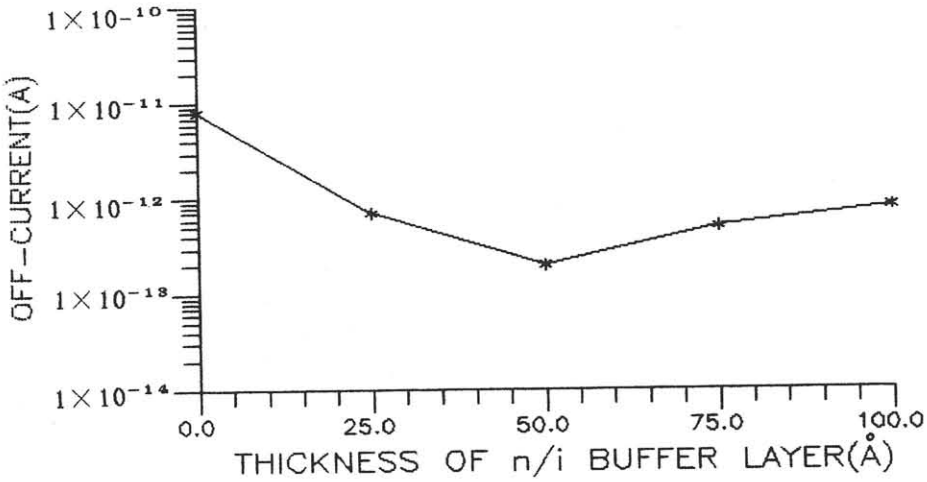

Fig.1 Plot of I_{OFF} vs the thickness d_B of the n/i buffer layer.

distribution by invoking the Poisson's equation.

It is shown that the electric field across the i layer with n/i buffer layer is high enough, and that at the n/i interface is enhanced by the n/i buffer layer, which is benefit to the motion of the electrons towards the source electrode and forbidden the injection of the holes towards the i layer and hence the channel. Therefore, the OFF-current induced by the hole-current is depressed by the n/i buffer layer.

On the behalf of the experimental results, the electric field was changed weakly for too thin and too thick buffer layer, which is obviously accord with the approach of our experimental outlines.

Based upon the view of energy band and material physics, it is suggested that the energy band at the n/i interface be graded, which is benefit to the movement of electrons towards the source electrode and block the hole movement towards the i layer. On the other hand, it is suggested that the n/i buffer layer deminish the lattice mismatch at the n/i buffer layer and hence reduce the dense generation-recombination center, which reduce the OFF-current of a-Si TFTs.

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