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Analytical Temperature-Rise Model for SOI MOSFETs

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A simple analytical model for temperature-rise in SOI MOSFETs is proposed. The model uses transfer-matrix representation for the heat flow out of the channel region. The temperature-rise calculated with the model shows a good agreement with temperature-rise evaluated from measurements of transient drain-current characteristics.

1 INTRODUCTION

Dielectric isolation of the channel region from the substrate gives SOI MOSFETs such attractive features as radiation hardness and small parasitic capacitance. However, owing to a small thermal conductivity of the buried oxide layer, SOI MOSFETs are susceptible to be heated up during their operation, resulting in reduction of output conductance. At a high power dissipation, the reduction becomes so large that a negative differential conductance is observed in $I_d - V_d$ characteristics [1,2]. Hence, an accurate SOI device simulation including self-heating effect is inevitable. Although this can be achieved numerically by including the thermal equation in a device simulation, it is worthwhile to have a simple analytical model to estimate the temperature-rise, which is the aim of this paper.

2 MODEL

In a steady-state operation of SOI MOSFETs, heat flows out of the channel into the substrate through the SOI layer and the buried oxide layer, as schematically shown in Fig. 1. Since the reduction in output conductance is significant in saturation regime where most of the power is dissipated at the drain edge, the heat source is assumed to be located at the drain edge.

The heat-flow is analyzed by decomposing the heat path into three regions, i.e., a) channel region, b) the region between the channel and the contacts, and c) contacts at the source and the drain. Temperature-rise ΔT and lateral heat-flux J at two boundaries of a region are related as

$$\begin{pmatrix} \Delta T_{i+1} \\ J_{i+1} \end{pmatrix} = M_i \begin{pmatrix} \Delta T_i \\ J_i \end{pmatrix}, \tag{1}$$

where heat-flux is assumed to flow from $i+1$ to i.

The transfer matrix M_i is expressed as follows:

(a) Channel region

$$M_2 = \begin{pmatrix} \frac{A+\beta(1-A)}{1-\beta(1-A)} & \frac{B}{1-\beta(1-A)} \\ \frac{C(1-2\beta)}{1-\beta(1-A)} & \frac{A+\beta(1-A)}{1-\beta(1-A)} \end{pmatrix} \tag{2}$$

A, B, C and β are expressed, respectively, as

$$A = \cosh(L/\Lambda') \tag{3}$$

$$B = \sqrt{R/(G+G')}\sinh(L/\Lambda') \tag{4}$$

$$C = \sqrt{(G+G')/R}\sinh(L/\Lambda') \tag{5}$$

$$\beta = \frac{G'\Lambda'\{\cosh(L/\Lambda')-1\}}{GL\sinh(L/\Lambda')+2G'\Lambda'\{\cosh(L/\Lambda')-1\}} \tag{6}$$

where L is effective channel length; Λ' is decay length of temperature-rise given by

$$\Lambda' = 1/\sqrt{(G+G')R}\,. \tag{7}$$

G, G' and R are expressed as

$$G = \kappa_{SiO_2} W/t_{box} \tag{8}$$

$$G' = \kappa_{SiO_2} W/t_{fox} \tag{9}$$

$$R = 1/\kappa_{Si} t_{SOI} W \tag{10}$$

where W is channel width; κ_{Si} and κ_{SiO_2} are thermal conductivity of silicon and SiO_2, respectively; t_{fox},

t_{SOI} and t_{box} are thicknesses of the front-gate oxide, the SOI layer and the buried oxide, respectively.

(b) Region between the channel and the contacts

$$M_1 = \begin{pmatrix} \cosh(\frac{L_N}{\Lambda}) & \sqrt{\frac{R}{G}}\sinh(\frac{L_N}{\Lambda}) \\ \sqrt{\frac{G}{R}}\sinh(\frac{L_N}{\Lambda}) & \cosh(\frac{L_N}{\Lambda}) \end{pmatrix} \quad (11)$$

L_N is length of the region; Λ is expressed as $1/\sqrt{GR}$; G is given by eq. (8); R is described as $1/\kappa_{Si}^{+} t_{SOI} W$ where κ_{Si}^{+} is thermal conductivity of n^+ (or p^+) silicon.

(c) Contacts

$$M_0 = \begin{pmatrix} 1 & 0 \\ GL_M & 1 \end{pmatrix} \quad (12)$$

L_M is the length of a metal contact.

The thermal conductance defined as

$$G_{th,\,i} = J_i/\Delta T_i \quad (13)$$

is calculated with a simple iterative procedure:

$$G_{th,\,i+1} = \frac{(M_i)_{21} + (M_i)_{22} G_{th,\,i}}{(M_i)_{11} + (M_i)_{12} G_{th,\,i}}, \quad (14)$$

together with the boundary condition of zero lateral heat-flux out of the contacts[3], i.e., $G_{th,\,0} = 0$.

The temperature-rise at the drain edge, ΔT_d, is calculated as

$$\Delta T_d = P/(G_{th,\,2} + G_{th,\,3}) \quad (15)$$

where P is the power dissipation at the drain edge. The temperature rise at the source edge is described as

$$\Delta T_s = \frac{\Delta T_d}{(M_2)_{11} + (M_2)_{12} G_{th,\,2}}. \quad (16)$$

3 MEASUREMENT OF TEMPERATURE-RISE

The temperature-rise in the channel region has been measured with transient drain-current characteristics. The devices used in the measurement are n-channel SOI MOSFETs with $W = 10\mu m$ and effective channel length in the range of $0.3 - 1.7\mu m$. The thicknesses of the front-gate oxide, the SOI layer and the buried oxide are 15 nm, 100 nm and 500 nm, respectively.

Figure 2 shows measurement configuration. Applied gate voltage is 4.5 V, which is large enough to form an inversion channel. A pulse voltage is applied to the drain. Transient drain current is measured with a voltage-drop across a load resistor connected to the source. The solid curve in Fig. 3 shows a typical example of transient drain-current characteristics. The broken curve represents a calculated transient current with the time constant for temperature-rise given by

$$\tau = \frac{t_{box}}{\kappa_{SiO_2}} \Big\{ \rho_{SiO_2} c_{SiO_2} (t_{top} + 0.5 t_{box}) + \rho_{Si} c_{Si} (t_{SOI} + \frac{L}{L + 2\Lambda} t_{poly}) \Big\} \quad (17)$$

where t_{poly} ($= 0.3\mu m$) and t_{top} ($= 0.6\mu m$) are thicknesses of the polysilicon gate and the passivation oxide; ρ_{Si}, c_{Si} and ρ_{SiO_2}, c_{SiO_2} are density and specific heat of silicon and SiO_2, respectively. Figure 3 demonstrates that the time constant of measured drain current is comparable to the calculated time constant. The transient characteristics are therefore attributed to the temperature-rise in the channel.

Figure 4 shows initial and steady-state drain currents obtained from the transient measurements. The figure shows that initial $I_d - V_d$ characteristics (solid circles) agree very well with the drain-current curve (solid line) calculated with an analytical model[4], suggesting a room-temperature operation of the device at the onset of a drain pulse.

Temperature-rise has been evaluated at each drain voltage so that the difference between the calculated drain currents (solid and dashed lines) equals the difference between the measured drain currents (solid and open circles). In the calculation, we have incorporated into the device model[4] both mobility and threshold voltage measured in the range of $300 - 450$ K. The temperature-rise thus obtained is shown in Fig. 5 as a function of power dissipation.

The solid circles in Fig. 6 are temperature-rise per unit power dissipation, which are evaluated from $\Delta T/\Delta P$ in saturation regime, as shown in Fig. 5. Compared with the curves calculated from eqs. (15) and (16), the measured temperature-rise agrees with the temperature-rise at the source edge. This means that drain current in saturation regime is determined by the non-saturation portion of the channel.

4 CONCLUSIONS

A simple analytical model to estimate temperature-rise of SOI MOSFETs has been proposed. Validity of the model has been confirmed by evaluating temperature-rise from transient drain-current measurements.

References

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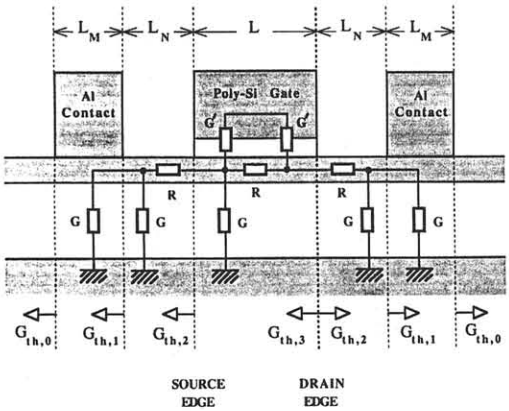

Fig. 1 Schematic representation of device structure. The heat-flow in the SOI layer and in the buried oxide are described with R and G, respectively.

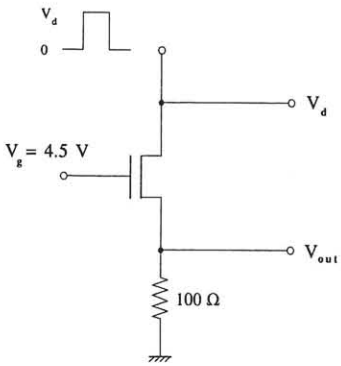

Fig. 2 Experimental setup for the measurement of transient drain-current characteristics.

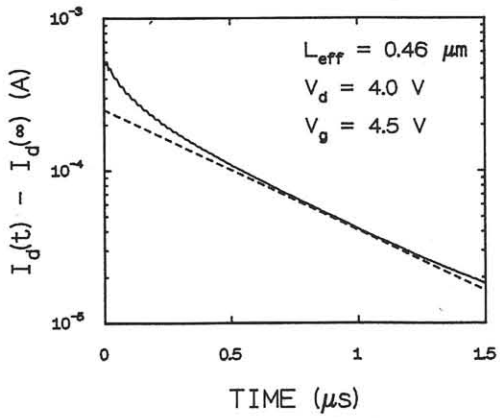

Fig. 3 Measured transient drain-current characteristics (solid curve) of an n-channel MOSFET with effective channel length of 0.46μm, together with calculated characteristics (broken line) by using eq. (17).

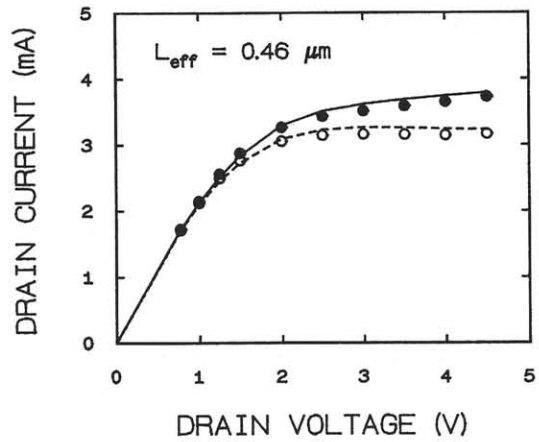

Fig. 4 Initial drain current (•) and steady-state drain current (o) measured as a function of drain pulse voltage. The solid curve shows drain current calculated with an analytical model[4] assuming no temperature-rise, while the broken curve includes temperature-rise.

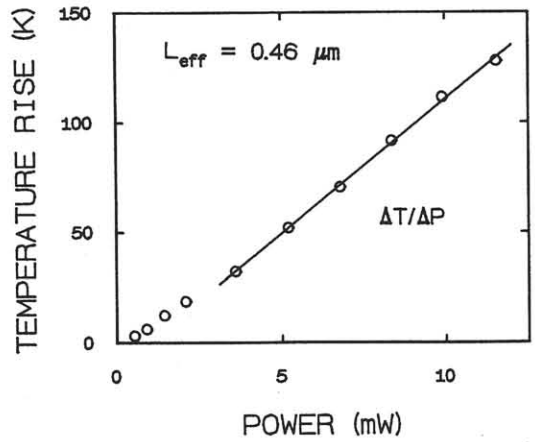

Fig. 5 Temperature-rise as a function of steady-state power dissipated in the channel.

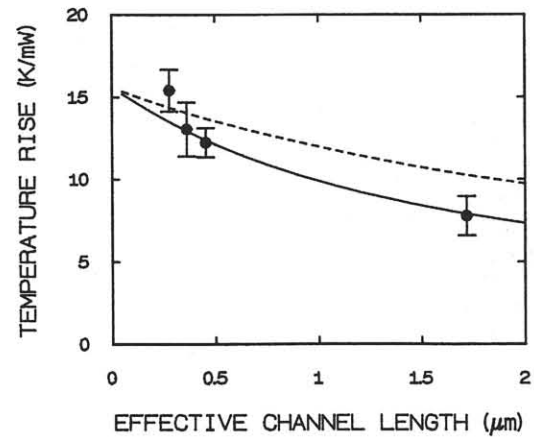

Fig. 6 Temperature-rise per unit power dissipation as a function of effective channel length (solid circles). Calculated temperature-rise at the source edge (solid curve) and the drain edge (broken curves) are also shown.