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Hot Carrier Reliability of Submicron Ultra Thin SOI-MOSFET's

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Hot carrier characteristics of ultra thin SOI-MOSFET's were examined. Floating substrate affects the hot carrier characteristics, in which body(substrate) current is observed at low gate voltage and the dependence of the hot carrier life time on drain voltage is different from that of conventional bulk MOSFET's. The shift of the transistor static characteristics after the stress is mainly observed as threshold voltage shift unlike bulk MOSFET's in which drain current shift is dominant. This is speculated to be due to electron injection to the underlying oxide of SOI structure.

Introduction

An ultra thin SOI-MOSFET is attractive for a basic transistor structure of deep submicron or further scaled dimensions due to its immunity from short channel effect. Since floating substrate effect which affected source-drain breakdown voltage lowering had been a problem in short channel thin SOI-MOSFET's, we adopted and optimized a gate overlapped structure¹⁾ for thin SOI-MOSFET's²⁾. Here it has become a important subject to investigate a hot carrier reliability of the short channel thin SOI-MOSFET³⁾ associated with the floating substrate effect and a underlying oxide which are unique in the SOI structure. In this paper, we investigated the hot carrier degradation behaviors in thin SOI-MOSFET's compared to bulk Si MOSFET's.

Experimental

Starting substrate was a SIMOX⁴) wafer, for which oxygen was implanted at an energy of 200keV and at a dose of 1x10¹⁸/cm², and high temperature annealing at 1300 °C was performed. Conventional CMOS process followed the substrate formation. Gate oxide, SOI and buried oxide thickness after processing were 15nm, 120nm and 300nm, respectively. Gate overlapped LDD structure was introduced to thin SOI-MOSFET's by oblique ion implantation technology. Self-aligned silicide process was used for reducing the resistance of the thin source and drain region.

Results and Discussion

Figure 1 shows the schematic cross section and dimension of the measured thin SOI-MOSFET's used in this study. Body electrode is introduced to some devices under a gate electrode. Figure 2 shows the hot carrier degradation as a function of the gate voltage. The maximum shift of threshold voltage was observed around Vg=1/2Vd and that of drain current was observed at a little bit lower gate voltage. Figure 3 shows the substrate current characteristics as a function of the applied gate voltage by using the four terminal SOI-MOSFET with a body contact. The maximum body (substrate) current was observed around Vg=1-2V and indicated plateau shape. This is





supposed to be due to the floating substrate effect occurred at low gate voltage region. Figure 4 compares the hot carrier degradation behavior of the threshold voltage and the drain current between the thin SOI-MOSFET and the bulk MOSFET. Although the drain current degradation was dominant in bulk MOSFET's, main issue in thin SOI-MOSFET's was the threshold voltage shift. Figure 5 shows the relationship between life time and supplied voltage of both structures. More abrupt change of the life time on drain voltage was found in thin SOI-MOSFET's than that in bulk Si devices. and at high drain voltage stress the life time of thin SOI-MOSFET's became much lower than that of bulk MOSFET's. Figure 6 shows the hot carrier life time for various drain structures. The hot carrier life time of thin SOI-MOSFET's was much improved by using LDD or gate overlapped LDD structure as compared to single drain structure. However, the curve of the life time became different from that of bulk MOSFET's. It could be also seen in the figure that the gradient of the curves for the LDD and the single drain structure gradually increased with increasing drain voltage. This implies that the hot carrier degradation mechanism in thin SOI-MOSFET's at high voltage region in which the floating substrate effect is supposed to be occurred was different from that at low voltage region and different from that in bulk MOSFET's.



Fig. 2 Hot carrier degradation of threshold voltage and drain current as a function of gate voltage.

Fig. 5 Relationship between hot carrier life time as a function of drain voltage.



Fig. 3 Body (Substrate) current of thin SOI-MOSFET as a function of gate voltage.



Fig. 4 Threshold voltage and drain current shifts as a function of aging time.



To confirm the main factor of the unique threshold voltage degradation, the back gate voltage dependences of the threshold voltage degradation was examined as shown in Fig. 7. The threshold voltage was degraded rapidly above the critical positive back gate voltage which assists electron injection to the back Si/SiO₂ interface. This indicates that the underlying oxide tend to be degraded easily as compared to the front gate oxide. Hence the electron injection to the back interface is supposed to be related with the degradation. Moreover, to distinguish the front and back interface effect, alternate electron and hole injection experiment was carried out. For one sample, first electron was injected to front gate oxide and secondly hole was injected (sample A). For the other sample(sample B), hole was injected for the first time and sequential electron injection was performed (Fig. 8). The threshold voltage was degraded at the channel hot electron injection step, however the compensation by the hole injection which was reported in bulk MOSFET's⁵⁾, was not observed in thin SOI-MOSFET's. By these results, the hot carrier degradation in thin SOI-MOSFET's is speculated to depend on the electron injection to the underlying oxide. In the fully-depleted thin SOI-MOSFET's, charge coupling is occurred by the fully-depleted condition in the body. Therefore, interface trap charges and/or oxide trap charges at the back Si/SiO₂ surface can affect the front channel threshold voltage easily as compared to the front channel carrier mobility or drain current.



Fig. 6 Drain structure dependences of the hot carrier life time in thin SOI-MOSFET's.

Fig. 8 Threshold voltage shift by alternate hot electron and hole injection to front gate oxide.

Conclusion

Hot carrier behavior in ultra thin SOI-MOSFET's was examined. The influence of floating substrate effects was observed in body current characteristics and the drain voltage dependences of the hot carrier life time. Threshold voltage shift is observed as a main degradation on the transistor static characteristics and is supposed to be due to the underlying oxide.

References

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Fig. 7 Threshold voltage shift as a function of back gate bias.

