Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials, Yokohama, 1991, pp. 660-662

Operation of Ultra-Thin-Film SOI/SIMOX pMOSFET's at Liquid Nitrogen Temperature

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Superior characteristics of ultra-thin-film SOI/SIMOX pMOSFET's at low temperature are presented. The suppression of short channel effect with decreasing temperature enhances, compared to bulk devices with the same channel doping. This result is explained by increase of effective channel length at low temperature. The carrier mobility at a low temperature increases more rapidly than that of bulk devices. The change of transconductance with hot carrier effect depends slightly on stress time. The initial degradation for SOI devices is larger.

1. Introduction

Compared with the bulk/MOSFET's, Silicon-on-Insulator (SOI) MOSFET's offer absence of latch-up, low parasitic capacitances and increase of packing density. Moreover, ultra-thin-film SOI/MOSFET's have several advantages such as suppression of short channel effect [1], increase of carrier mobility [2], and excellent subthreshold slope [1], especially when they are operated in a fully depleted mode .

On the other hand, scaled down MOSFET's need reduction of supply voltage to keep the reliability of devices, which leads to low temperature operation in order to obtain on/off margin of gate voltage. It is well known that operation at low temperature is effective in order to keep long-channel device behavior of MOSFET's [3].

In this paper we report several superior characteristics of ultra-thin-film SOI/SIMOX pMOSFET's at liquid nitrogen temperature (LNT).

2. Experimental

SOI wafers were prepared by SIMOX with the following processing. O^+ was implanted into p-type, 100Ω cm, (100) Si substrate at an energy of 200KeV and a dose of $2.4\times10^{18}cm^{-2}$, followed by 6 hours annealing at 1315C in Ar/O_2. These SIMOX wafers have SOI films of 80-100nm and buried oxide of 520nm, which was confirmed by using a multilayer optical spectroscopic ellipsometry and a TEM.

PMOSFET's, with a channel width of 20μm and a gate oxide of 10nm, were fabricated on the SIMOX wafers. LOCOS isolation is used in the MOSFET's. Phosphorus was doped in the channel region with concentrations of 2×10^{16}-$2\times10^{17}cm^{-3}$. Bulk MOSFET's were also fabricated on n-type, 10 Ω cm, (100) Si wafers with the same device processing and channel control doping. The junction depth X_j of bulk MOSFET's, which is estimated by process simulation, is about 0.35μm. The effective channel length L_{eff} is obtained by using Laux method [4].

Characteristics of both SIMOX and bulk MOSFET's were measured at temperatures of 90, 150, 200, 250, and 295K(room temperature).

3. Result & Discussion

Subthreshold Characteristics

I_d-V_{gs} characteristics of SOI devices with a SOI film of 80nm, a channel length of 10μm, a channel doping of $2\times10^{16}cm^{-3}$, and a drain voltage of -5V, are shown in Fig. 1.

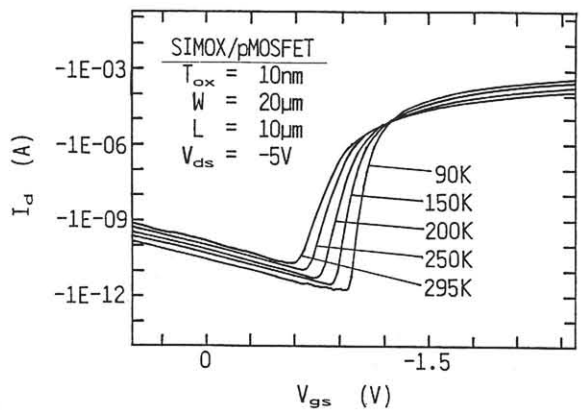


Fig. 1 I_d-V_{gs} characteristics as a function of temperature.

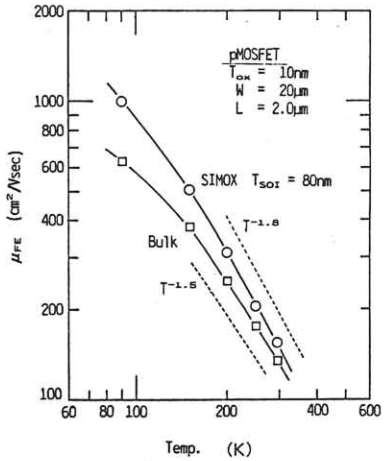


Fig. 2 Field effect mobility for SIMOX and Bulk pMOSFET.

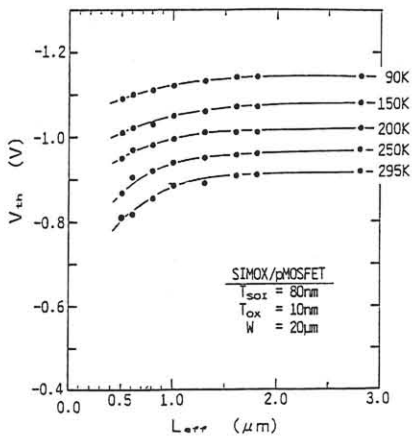


Fig. 3 Threshold voltage for SIMOX pMOSFET as a function of temperature.

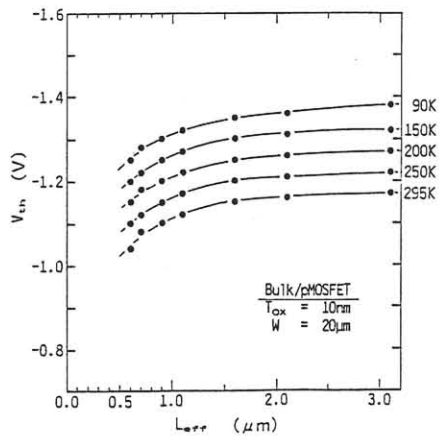


Fig. 4 Threshold voltage for Bulk pMOSFET as a function of temperature.

With decreasing temperature, subthreshold region is shifted toward enhancement side due to the change of Fermi level and the subthreshold swing is reduced from 62 to 22mV/decade. Leakage current in off-state has a constant slope with V_{gs}. Considering that the gate oxide is very thin and the leakage current slope is independent of temperature, we think that the off-state leakage current originates from band-to-band tunneling.

Carrier Mobility

Fig. 2 shows the dependence of field effect mobility μ_{FE} on temperature, which is extracted from transconductance g_m in a triode region(V_{ds}=-0.1V) of devices with a channel doping of $2x10^{16}cm^{-3}$. μ_{FE} of SOI and bulk devices increases from 155 and 130cm^2/Vs at 295K to 1000 and 630cm^2/Vs at 90K, respectively. Assuming that μ_{FE} is proportional to T^{-x}, x is 1.8 for SOI devices and 1.5 for bulk devices, indicating that larger μ_{FE} can be obtained for SOI devices than bulk devices at a lower temperature. It is shown from the calculation based on a simple 1-D model that the total charge for SOI devices which is induced to form an inversion layer is less than half of that for their bulk counterparts. Therefore, the electric field perpendicular to MOS interface, which degrades μ_{FE}, is weaker in SOI devices than in bulk devices. This tendency becomes more notable as temperature decreases, which supports the present experimental results.

Short Channel Effect

L_{eff} dependences of threshold voltage for SOI and bulk devices with a channel doping of $2x10^{16}cm^{-3}$, are shown in Fig. 3 and Fig. 4, respectively. It is clearly shown that, with decreasing temperature, the short channel effect is enormously suppressed in SOI devices, whereas is independent of temperature in bulk devices.

This result can be explained by considering the temperature dependence of L_{eff} for SOI and bulk devices. Fig. 5 shows the experimental result of L_{eff} as a function of temperature, indicating that L_{eff} increases by 0.40μm in SOI devices, on the other hand, by 0.08μm in their bulk counterparts with decreasing temperature from 295K to 90K.

Fig.6 shows the temperature dependences of L_{eff} as a function of channel doping. Bulk devices without channel doping show a noticeable increase of L_{eff} at LNT. SOI devices with a high channel doping show only a slight increase of L_{eff} at LNT. However, it should be emphasized that short channel effects are suppressed much more for SOI devices than their bulk counterparts at LNT, if both devices have the same channel doping.

The suppression of short channel effect at LNT can be explained based on the amount of channel doping. The shift of Fermi level with temperature, ΔE_f, is larger in Si with a lower doping. Depletion layer thickness in MOS is dependent on change of surface potential, $2\Delta E_f$. On the other hand, depletion layer thickness in p^+-n^- junction depends on ΔE_f, assuming that Fermi level of p^+-Si is independent of temperature. Therefore, for devices with a low channel doping, the gate dominates channel region more effectively at low temperature than at room temperature [3].

Moreover, as X_j is decreased, the short channel effect is more suppressed. The X_j for SOI devices (80-100nm) is much shallower than that for bulk devices (350nm).

Hot Carrier Effect

Hot carrier effects are studied for both devices with a channel doping of $2x10^{17}cm^{-3}$. Since substrate current can not be monitored easily for SOI devices, we choose the stress

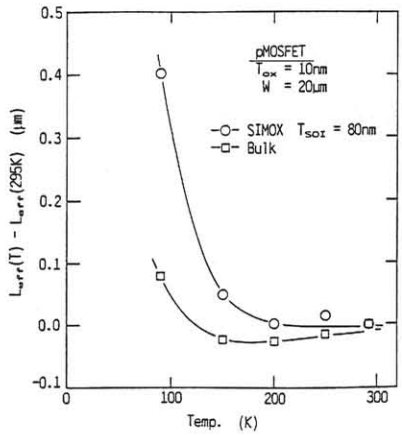
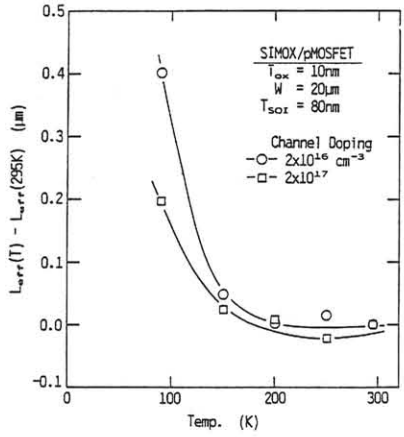
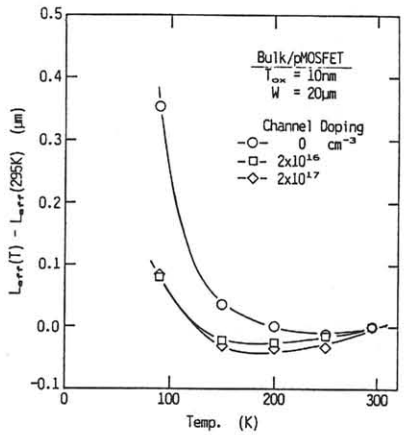


Fig. 5 Temperature dependence of effective channel length for SIMOX and Bulk pMOSFET.





(a) SIMOX pMOSFET (b) Bulk pMOSFET

Fig. 6 Temperature dependence of effective channel length as a function of channel doping.

condition that the gate current I_g is maximum with V_{ds}=-6.5V. Polarity of I_g shows that it is composed of electron. Changes of g_m with stress time, $\Delta g_m/g_{m0}$, at 295 and 90K, are shown in Fig. 7. Since fixed negative charges are produced in the gate oxide by electron injection, g_m in both devices increases after stress.

$\Delta g_m/g_{m0}$'s for SOI devices at both room temperature and LNT, are larger than those for bulk devices. $\Delta g_m/g_{m0}$'s depends slightly on stress time. The initial degradation for SOI devices is about 10%. This indicates that lower supply voltage is needed for SOI devices at LNT.

Although maximum I_g's for both devices, are larger at room temperature than at LNT, $\Delta g_m/g_{m0}$'s have the opposite trend. The shift of threshold voltage at LNT is smaller than that at room temperature. This indicates that the amount of fixed charge at LNT is lower than that at room temperature. Judging from these results, we suppose that fixed negative charges in the gate oxide affect more strongly carrier transport in MOS structure at LNT.

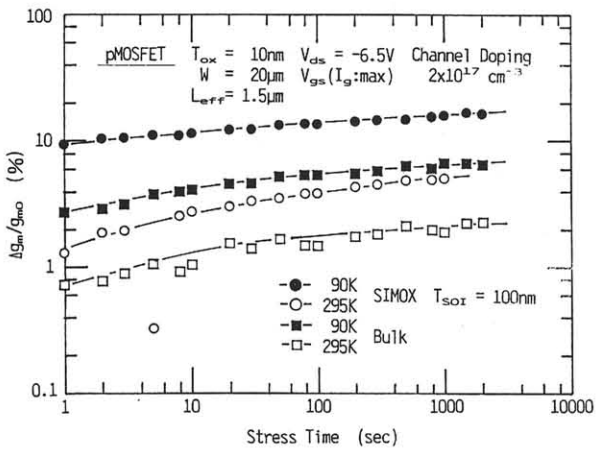


Fig. 7 Stress time variation for change of transconductance for SIMOX and Bulk pMOSFET.

4. Conclusion

Low temperature characteristics of ultra-thin-film SOI/pMOSFET's have been intensively studied. The suppression of short channel effect is enhanced with decreasing temperature, compared to bulk devices with the same channel doping. The carrier mobility at low temperature increases more rapidly than that of bulk MOSFET's. If the supply voltage is reduced, ultra-thin-film SOI devices would be a promising candidate for deep-submicron MOSFET's at low temperature .

References

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