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Internal Barrier Height Lowering Due to Grain Boundary Charge Repopulation in Polycrystalline Silicon

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Non-ohmic and time-dependent conductance behaviors have been studied in moderately doped polycrystalline silicon. We found that it is difficult to be explained by the conventional model which does not include the change of Fermi level in grain boundary, and that these phenomena are closely related to each other. To explain the experimental results, we propose a new model which takes into account the internal barrier height lowering due to charge detrapping in grain boundaries.

1. INTRODUCTION

Polycrystalline silicon (poly-Si) is a material of great interest for thin-film transistors as well as passive resistors. However, these device-performances depend not only on the device structures, but also strongly on the electrical properties of poly-Si itself.

Electrical properties of poly-Si have been usually explained by charge trapping and thermionic emission model. The current is limited by grain boundary potential barrier formed by the carriers trapped at the grain boundary interface states. Although this model is quite successful to describe small-signal theory, it does not explain non-ohmic behavior usually observed in lightly and moderately doped poly-Si.

In the present work, we have focused on the non-ohmic behavior and the transient response of the conductance in moderately doped samples to investigate the characteristics inherent in the poly-Si.

2. SAMPLE PREPARATION AND MEASUREMENTS

Poly-Si resistor bars with the width of, 1.5, 5, 10 μm and the length of 400 μm were fabricated on 0.4 μm-thick LPCVD poly-Si. Phosphorous doses ranging from 4×10^{12} to 4×10^{15} cm^{-2} were implanted, and annealed at 900C for 30 min in N_2 ambient to remove the implantation damages and to ensure the uniform distribution.

The current-voltage (I-V) characteristics and the transient response of the conductance were measured using two-probe method, since the contact resistance was negligibly small compared with poly-Si resistance.

3. RESULTS AND DISCUSSION

3-1 Non-ohmic behavior

Figure 1 shows the I-V characteristics of the moderately doped samples (4×10^{12} cm^{-2}) with W=10 μm. Significant non-ohmic behavior is observed above 6 V.

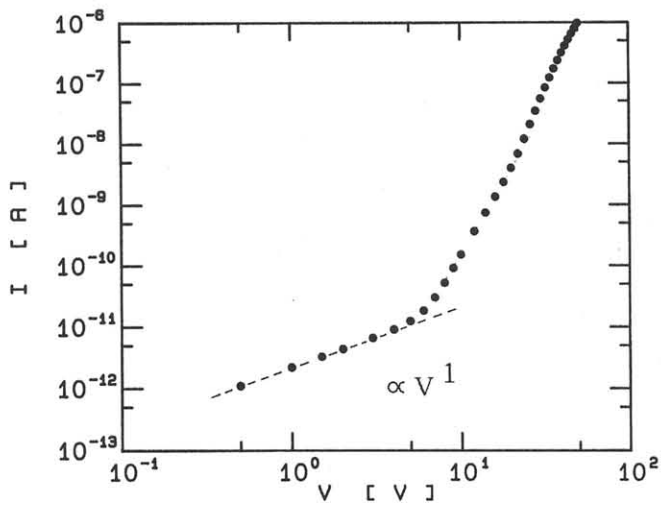

Fig.1 log I vs. log V plot for $4\times10^{12}cm^{-2}$ P dose, W/L=10/400 μm sample at room temperature.

In Figure 2, applied voltage dependence of relative conductance, σ/σ_0 , is shown together with the calculated curve based on Lu's model[1]. It clearly shows that the strong non-linearity cannot be reproduced by Lu's model which is based upon the simple thermionic emission assuming that the voltage across the barrier is equally divided on each side of the junction and that the barrier height measured from Fermi level in the boundary is unchanged.

Moreover, it has been found that non-linearity becomes stronger for narrower samples. Since the ratio of surface area to volume is larger for narrower samples, the Joule-induced heating should be smaller for narrower samples. Therefore, this experimental result cannot be explained by simple Joule-induced heating which has been attributed to a cause of non-linear conductance in undoped poly-Si[2].

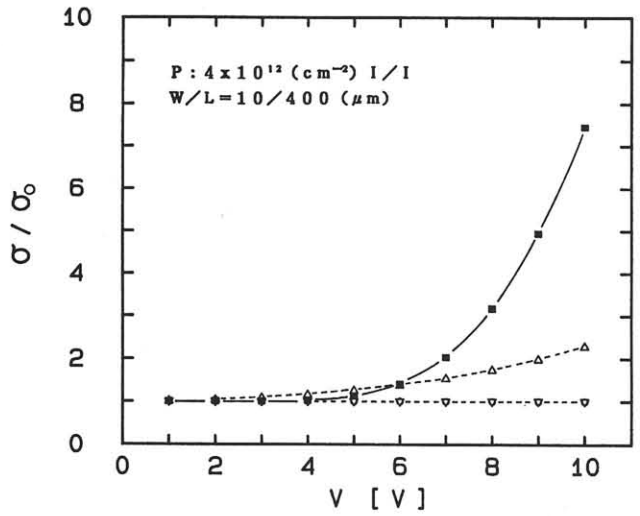

Fig.2 Measured (■)and calculated (○,▽,△) σ/σ_0 - V characteristics. Calculation is based on Lu's model with grain size 500A(○),5000A(▽) and 5 μm(△). Here, σ_0 denotes the conductivity in ohmic region.

3-2 Transient response

Figure 3 shows the time response of the transient current at 300K as a parameter of the applied voltage. These bias-dependent transient responses cannot be explained by a RC delay in the grain boundary network in the sample. With increasing temperature, the rise time was sharply shortened.

In addition, we noticed that the non-ohmic behavior was correlated very well with the transient response, as shown in Figure 4. This suggests that non-ohmic behavior and transient response have a same origin inherent in poly-Si.

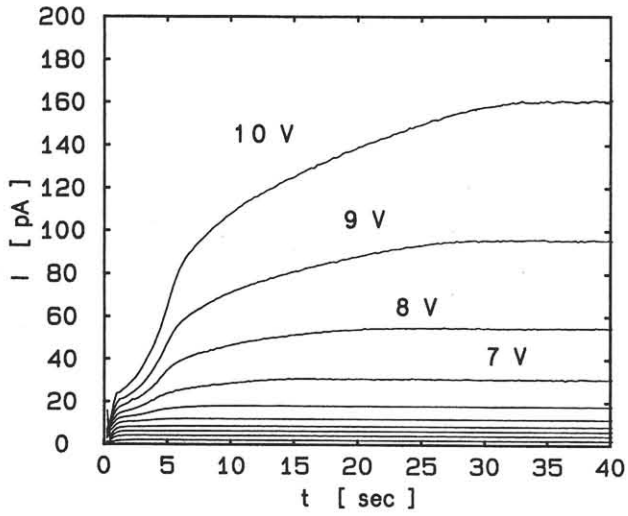

Fig.3 Transient current observed for various voltages for W/L=10/400 μm at room temperature.

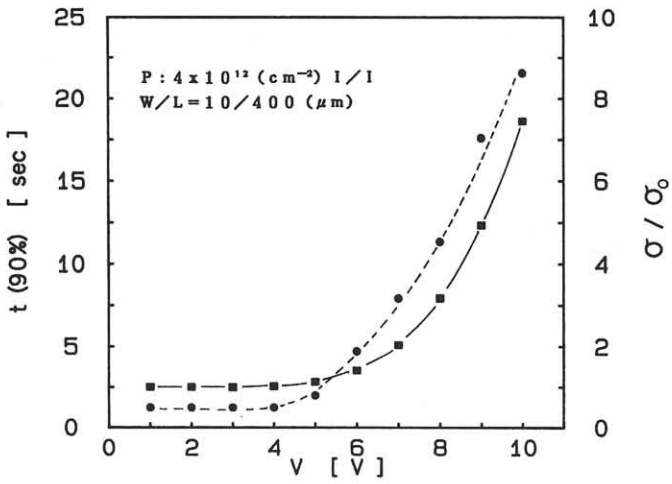

Fig.4 Correlation between voltage dependences of rise time (●) and of relative conductivity(■). Rise time is defined as the time when the current reaches 90% of the stationary current.

3-3 Internal barrier height modulation model

To interpret the experimental results, we present a new model in which both results can be reasonably explained. The basic idea is that total charges trapped at the grain boundaries vary with the applied bias. It means that the local barrier height at the grain boundary, qV_B, depends on the applied

bias, because the charge redistribution should be brought about by the local field. It is practically impossible to determine the modulated barrier height self-consistently, so we have newly incorporated the bias-dependent barrier height component, $q\Delta V_B$, at the grain boundary into the thermionic emission model.

$$I(V)=A^*T^2 \exp[-(qV_B^*+\zeta)/kT] \sinh(qV/2kT)$$

Here, A^* denote the Richardson constant, $V_B^*=V_{Bo}+\Delta V_B$ and ζ is the energy difference between conduction band and Fermi level inside the grain. As shown in Figure 5, the applied bias dependence of ΔV_B was determined to fit the results in Figure 2. In the present sample, the internal barrier height lowering at a grain boundary is about 40 meV when 10 V was applied to the sample.

The fact that the activation energy of the stationary current is lowered by increasing applied bias, as shown in Figure 6, is another experimental evidence that the internal barrier height is lowered at the grain boundary.

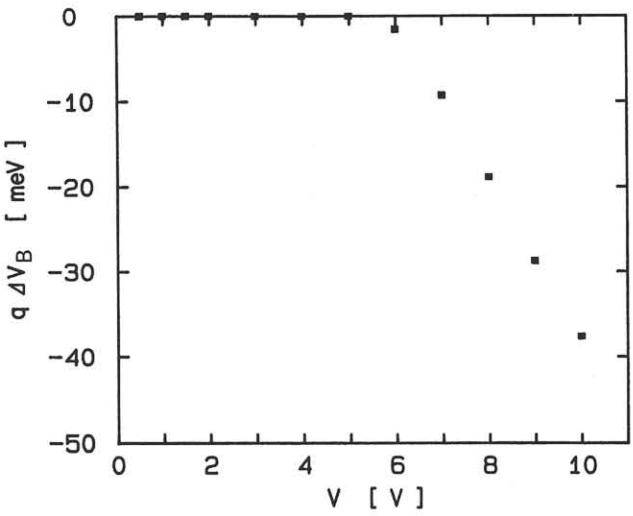

Fig.5 Voltage dependence of calculated barrier height modulation $q\Delta V_B$ at room temperature.

4. CONCLUSION

The non-ohmic and transient behavior of the conductance observed in moderately doped poly-Si was experimentally investigated and it was found that they are closely related each other. Based upon the results, a new model with internal barrier height lowering due to charge detrapping at the grain boundary interface states have been proposed. This consideration is required to describe I-V characteristics precisely. And, the transient measurement can be a useful method to evaluate the grain boundary electrical properties.

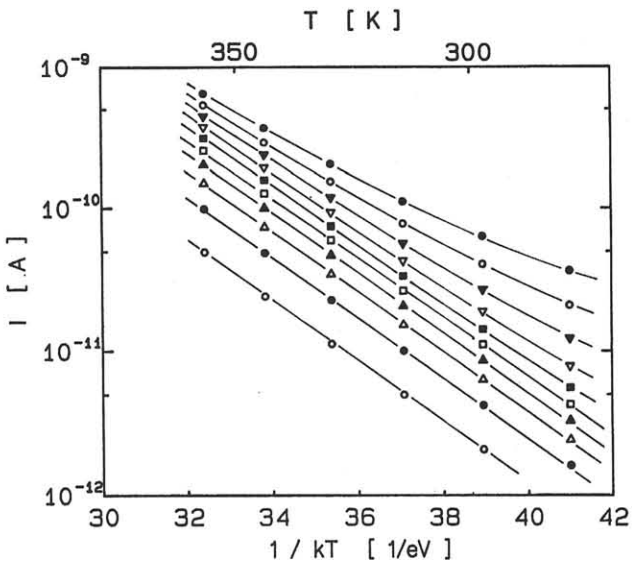

Fig.6 Temperature dependence of stationary current for various applying voltages.

REFERENCES

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[1] N. C. C. Lu et al., IEEE ED-28(1981) 818.
[2] C.A. Dimitriadis, J. Appl. Phys. 68(1990) 862.