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A Proposal of a Highly Sensitive Interline CCD for HDTV

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We propose new device structures for an interline CCD for HDTV, and analyze their performance in a 2-million-pixel image sensor with a 1-inch image format. The offset-shallow p^+-isolation and the completely-depleted well make it possible to shrink the channel width of the vertical CCD by 40% maintaining a charge handling capability of 22 fF. The combined use of a tetrode transistor and fluorine implantation reduces the noise charge of the amplifier by about half. These results indicate that the interline CCD has potential for HDTV applications.

1. INTRODUCTION

A solid-state imaging device for high-definition TV systems needs to have 5 to 8 times as many pixels as conventional devices.[1)2)] This requirement, in conjunction with the need for miniaturization, makes it necessary to reduce the pixel size. However, in an interline CCD,[1)6)] which is widely available on the market, the area of the vertical CCD cannot be scaled down without sacrificing charge handling capability, and enlarging the signal band increases random noise of the output amplifier.

We propose new device structures to increase the charge handling capability of the vertical CCD and to lower the random noise of the amplifier. Their performance in a 2-million-pixel image sensor with a 1-inch image format is compared to a conventional structure.[6)]

2. CHARGE HANDLING CAPABILITY

The maximum charge that can be transferred through the vertical CCD (charge handling capability) Q_S is given by:

$$Q_S = C_U L(W-\Delta W)V \qquad (1)$$

where C_U is the capacitance per unit area, L is the channel length, W is the channel width, ΔW is the narrow channel factor, and V is the pulse swing. Pixel size reduction reduces the vertical CCD area.[3)] Therefore, there are only two ways to maintain the charge handling capability with a constant pulse swing; to decrease ΔW or to increase C_U.

A cross-sectional view of the proposed vertical CCD is shown in Fig.1. In this structure, the shallow p^+ and p^- double well isolates the n CCD channel from the n photodiode.[4)] There is no deep p-isolation in this structure. The shallow p^+ is offset by only 0.3 μm from the n CCD channel. As a result, the narrow channel factor is lowered without degrading the isolation. Moreover, the n CCD channel is shallowed to the minimum possible with the process in order to increase the unit capacitance. The results of a two-dimensional computer simulation of the charge handling capability

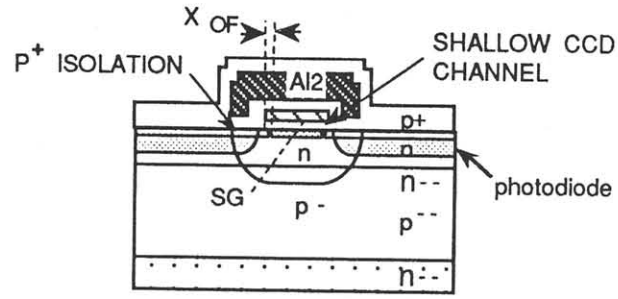

Fig.1 Cross-section of the vertical CCD isolated by the shallow p^+ layer

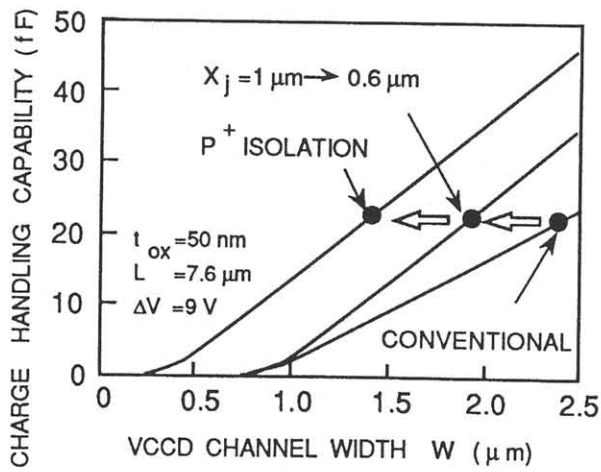

Fig.2 Charge handling capability of the vertical CCD

are shown in Fig.2. The proposed structure, with a channel 0.58 times as narrow as the conventional device, has the charge handling capability of 22 fF, which is satisfactory for operation.

Shallowing the CCD channel inevitably degrades the charge transfer efficiency of the horizontal CCD, which has the same doping profile as the vertical CCD. This problem has prevented the shallowing of the CCD channel in conventional devices. Moreover, a CCD for HDTV needs 3 to 4 times faster charge transfer.

Charge transfer inefficiency is approximately proportional to the single-carrier transient time t_{tr}, which is given by:

$$t_{tr}=L/2\mu E_{fm} \quad (2)$$

where μ is the electron mobility and E_{fm} is the minimum fringing field.[3] Hence, a higher minimum fringing field is necessary to achieve faster charge transfer. The completely depleted well structure shown in Fig.3 enhances the minimum fringing field. In this structure, the n^{--} well is formed under the p^{-} double well of the horizontal CCD. The depletion layer is about 4 times as deep as in the conventional one. The results of two-dimensional computer simulation of the minimum fringing field are shown in Fig.4. When the well is not completely depleted, the minimum fringing field is 2/3 the conventional one because the channel is shallow. However, it reaches 7 times when the well is completely depleted (when well potential is over 0 V). This value is sufficient for the HDTV CCD.

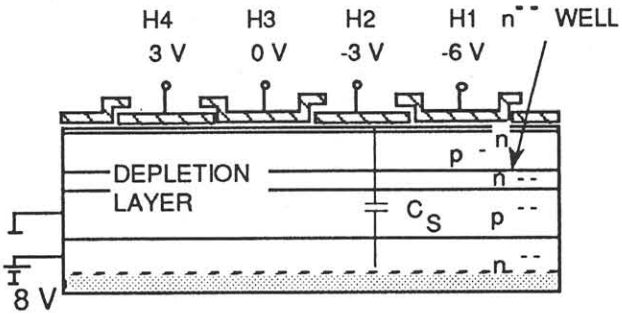

Fig.3 Cross-section of the horizontal CCD with a completely depleted well

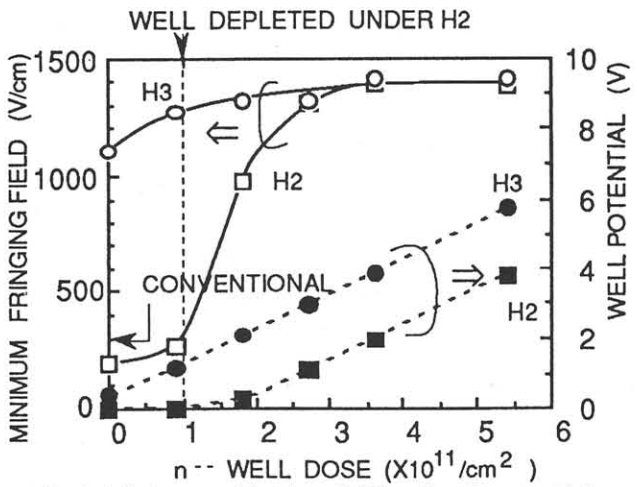

Fig.4 Minimum fringing field and well potential

3. RANDOM NOISE

The schematic diagram of the output amplifier is shown in Fig.5. In this configuration, the primary noise source, after CDS (Correlated Double Sampling),[5] is the MOS driver transistor of the first source-follower. The random noise charge Q_n is given by

$$Q_n = \frac{C_{in}}{q}\sqrt{\frac{2f_{BO}}{f_H}\int_0^{f_B} 4\sin^2(\pi f T_S)\, S(f)\, df} \quad (3)$$

In equation (3), q is the electronic charge, Cin is the input capacitance of the amplifier, f_{BO} is the signal band-width, f_H is the driving frequency of the horizontal CCD, f_B is the cutoff frequency of the amplifier, Ts is the sampling period of the CDS circuits, and S(f) is the noise power spectrum. Increasing signal band-width increases of f_B and Ts. Therefore, S(f) and Cin need to be lowered.

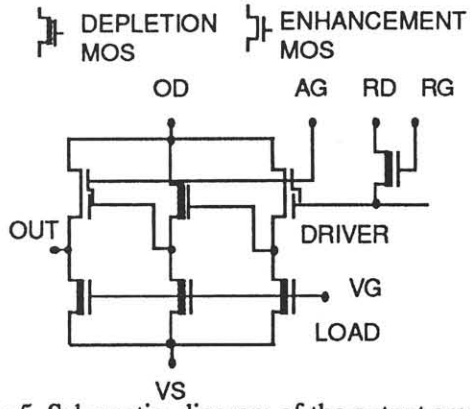

Fig.5 Schematic diagram of the output amplifier using tetrode transistors

A MOS transistor has two noise sources; thermal noise and 1/f noise. The power spectrum of thermal noise is inversely proportional to the ratio of the channel width to channel length. The power spectrum of 1/f noise is inversely proportional to the channel area. Accordingly, S(f) can be reduced by using a wide channel. In the case of the driver, however, the input capacitance of the amplifier C_{in}, which includes the gate capacitance of the driver, increases as the channel width increases. So, a minimum random noise charge is reached at the point where the gate capacitance of the driver C_G is equal to the parasitic capacitance at the input of the amplifier C_P. The thermal noise power spectrum can be reduced as the channel length decreases in order to increase mutual conductance. However, the breakdown voltage limits the use of a short channel. The tetrode transistor, shown in Fig.6, solves this problem. The constantly biased gate

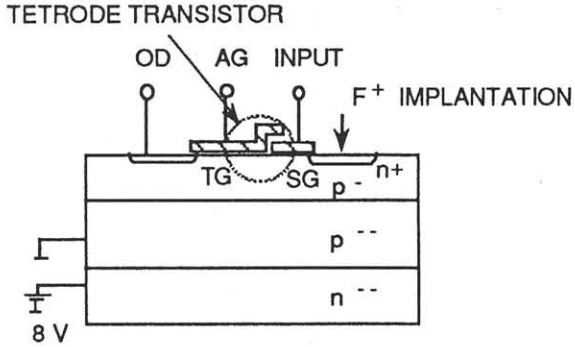

Fig.6 Cross-section of the tetrode transistor

AG shields the electric field from the drain (OD) in order to increase the breakdown voltage. The mutual conductance of the tetrode transistor increases as the effective channel length decreases, in the same way as the conventional one, as shown in Fig.7. The effective channel length at which the breakdown voltage reaches 7 V is less than 1 μm in the tetrode transistor and about 2.5 μm in the conventional one, as shown in Fig.8. Hence, the mutual conductance is increased three to four times for the same gate capacitance.

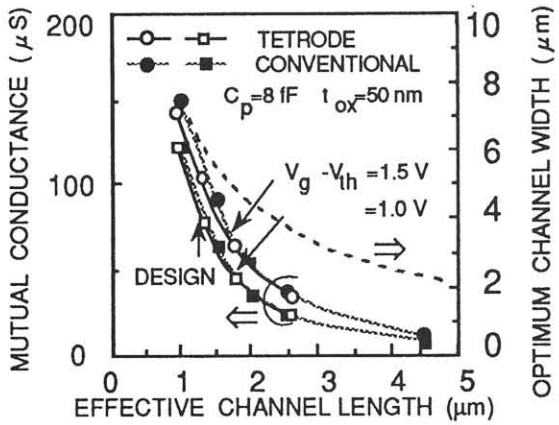

Fig.7 Mutual conductance of the driver with the optimum channel width

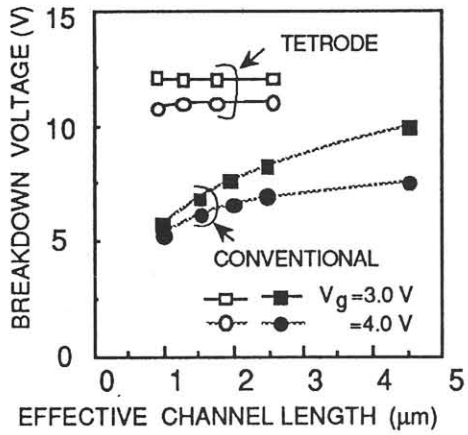

Fig.8 Breakdown voltage

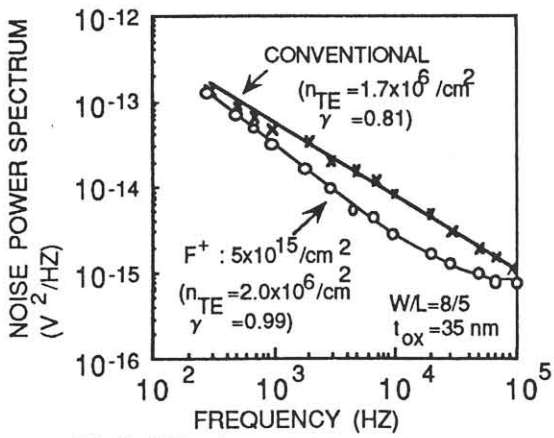

Fig.9 1/f noise power spectrum

Fluorine ion implantation [7] can reduce 1/f noise, as shown in Fig.9, because it inactivates the surface traps which generate 1/f noise.

The calculated total noise charge is shown in Fig.10. The new structure roughly halves the noise charge.

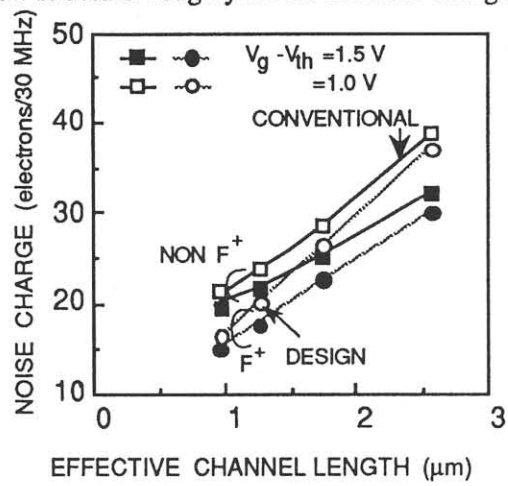

Fig.10 Noise charge of the output amplifier

4. CONCLUSION

The proposed device structure with the shallow p^+ isolation and the completely depleted well makes it possible to shrink the channel width of the vertical CCD by 40% while maintaining the high charge-handling capability. The combined use of tetrode transistor and fluorine implantation roughly halves the noise charge. These results indicate that the interline CCD has potential for HDTV applications.

5. ACKNOWLEDGEMENTS

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