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In-situ Doping of Epitaxial Silicon by Low-Temperature LPCVD for the Fabrication of Delta-Doped MOSFETs

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A low-temperature process has been investigated for the fabrication of delta-doped MOSFETs. The main process steps consist of a low-pressure chemical vapor deposition (LPCVD) at low temperatures and a wet oxidation at 700°C. By this process delta-doped n-channel MOSFETs have been fabricated and compared with conventional ones, containing a homogeneously doped channel layer. It is found that short channel effects can be suppressed by this delta-doped layer.

1. INTRODUCTION

With decreasing feature size of deep submicron MOSFETs, short channel effects increasingly influence the performance of the devices. Some of the most severe short channel effects are the drain induced barrier lowering (DIBL), affecting the output and subthreshold behavior, and punch through, leading to a gradual or, in the case of punch through, total loss of gate control. Among various approaches to overcome short channel effects, the delta-doped or atomic layer doped (ALD) MOSFET[1,2] is one of the most promising ones. In this device, a heavily doped thin epitaxial layer is formed below the channel region close to the surface, which prevents the space charge region of the drain from penetrating the channel. However, the realization of such a doping profile with a delta-doped layer became possible only recently with the development of low-temperature growth of high quality epitaxial layers. In addition, the overall temperature budget of the process has to be kept as low as possible to avoid a broadening of the delta-doped layer due to diffusion at elevated temperatures.

In this paper we investigated a low-temperature process for the fabrication of delta-doped n-channel MOSFETs. The structure of the delta-doped MOSFET is shown schematically in fig. 1. The process steps consist of epitaxial growth of the in-situ doped active region by low-pressure chemical vapor deposition (LPCVD)[3,4] at a temperature of 650°C, wet oxidation at 700°C for the gate oxide, arsenic implantation for the source and drain regions and phosphorous doped polysilicon deposition for the interconnects. The in-situ doping of the epitaxial silicon layers with boron has been investigated, depending on the temperature and the partial pressure of B_2H_6 in order to find the optimum process conditions for the delta-doping.

2. RESULTS

In order to control the epitaxial growth of in-situ doped silicon layers, we investigated the boron concentration and the deposition rate in the temperature range between 600 and 750°C. For the growth of delta-doped layers the boron concentration should be controlled over a wide range and

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the deposition rate should be maintained at a reasonably low value. Among various deposition conditions the best compromise has been found for a temperature of 650°C, where the doping concentration as well as the deposition rate can be well controlled. In fig. 2 the resulting electrically active boron concentration as a function of the B_2H_6 partial pressure is shown for the substrate orientations (100) and (111). The doping concentration can be varied in the wide range between 10^{16} and $10^{20}cm^{-3}$ necessary to grow boron spikes with a peak concentration close to $10^{13}cm^{-2}$ sandwiched between low doped layers. The corresponding silicon growth rate is shown in fig. 3 as a function of the B_2H_6 partial pressure. Utilizing these results delta-doped layers have been deposited with a thickness of about 150Å, as shown by the SIMS result in fig. 4. In contrast to the result in fig. 4, a symmetric shape of the boron spike can be obtained by an appropriate gas switching between the different doping levels.

For the gate oxide formation several oxidation conditions have been investigated at temperatures of 800 and 700°C. However, a wet oxidation at 700°C has been chosen in order to minimize broadening of the delta-doped layer. It has been found that the boron spike is not influenced by annealing in N_2 atmosphere carried out for 8 hours, whereas thermal oxidation even at 700°C may be crucial due to generation of point defects. Boron diffuses mainly due to the strong coupling between the boron atoms and these point defects.

By this process delta-doped and conventional MOSFETs with channel lengths in the range between 10.5 and 0.6µm have been fabricated, and their electrical characteristics are compared. The comparison of the I-V characteristics of both devices is shown in figs. 5 and 6. The low breakdown voltage of the delta-doped MOSFET is caused by the position of the boron spike in a depth of about 0.15µm, just below the source/drain junctions, which has a penetration depth of 120nm. This n^+-p^+ junction causes a high avalanche generation rate even at moderate drain voltages. By comparing the threshold voltages as a function of the channel length it is found that short channel effects can be reduced by delta-doped layers. Below 1µm the threshold voltage of the conventional transistor decreases, whereas that of the delta-doped MOSFET remains approximately constant. However, the threshold voltage of the delta-doped transistor is increased to unpractical values due to a compression of the depletion layer by the high doping concentration of the boron spike.

3. CONCLUSIONS

A low-temperature process consisting of in-situ doped epitaxial silicon growth by LPCVD at 650°C and a wet oxidation at 700°C has been presented which allows the fabrication of delta-doped devices. The doping concentration obtained by the LPCVD process can be controlled over a wide range. As an example delta-doped MOSFETs have been fabricated and compared with homogeneously doped transistors made by the same process. It is found that the delta-doped layer can be used to suppress short channel effects. However, the process has to be improved with respect to the thermal oxidation, and with respect to the location of the source and drain junctions.

4. REFERENCES

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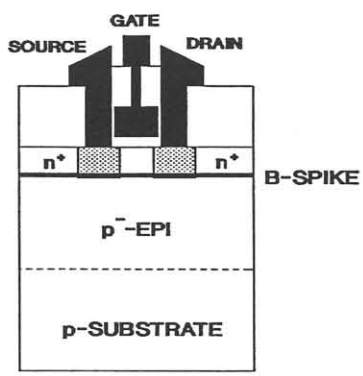

Fig. 1 Structure of the delta-doped MOSFET

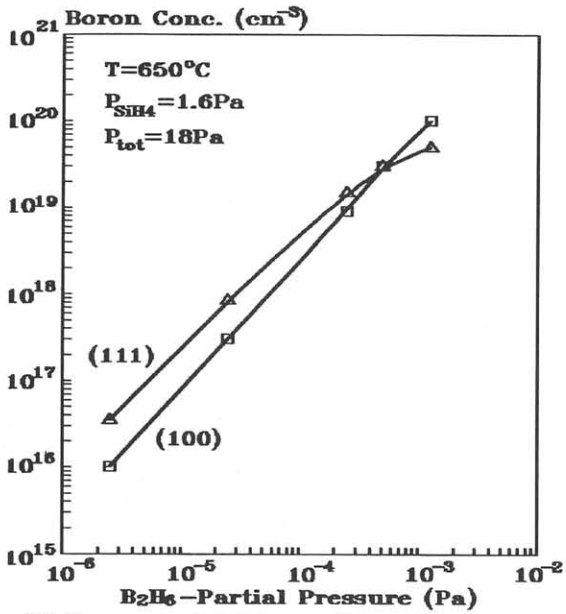

Fig. 2 B_2H_6 partial pressure dependence of the boron concentration

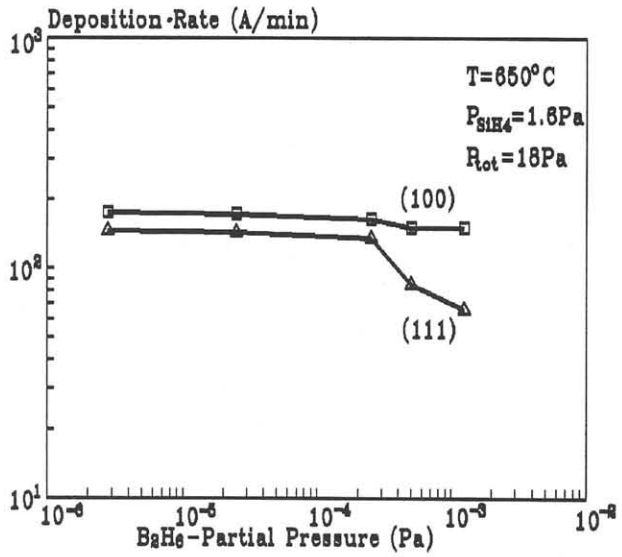

Fig. 3 Silicon growth rate as a function of the B_2H_6 partial pressure at 650°C

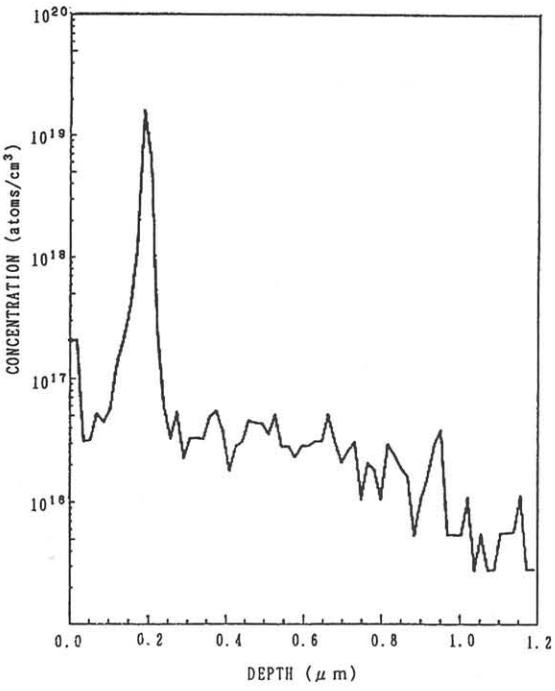

Fig. 4 SIMS results of the boron spike after deposition

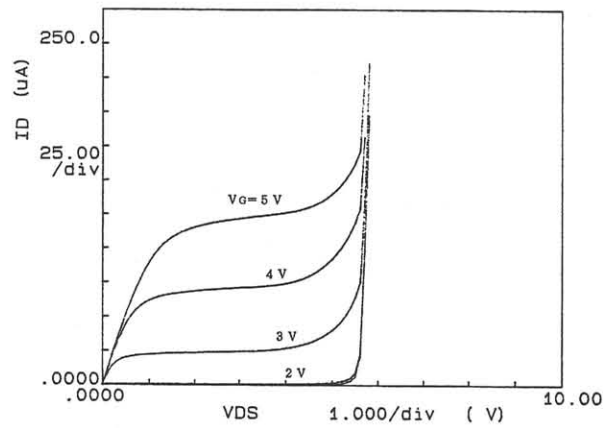

Fig. 5 I-V characteristics of the delta-doped MOSFET

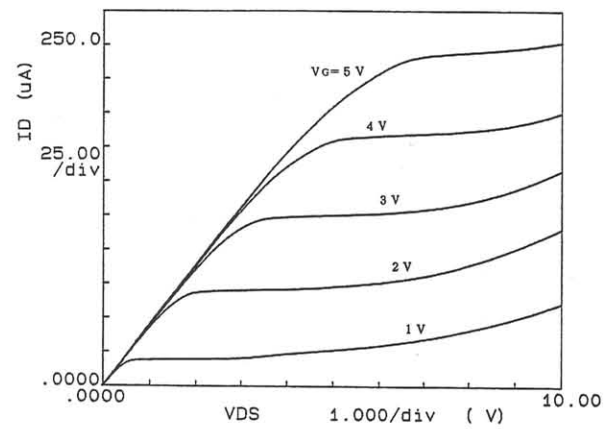

Fig. 6 I-V characteristics of the conventional MOSFET