Invited

High Performance Poly-Si TFT for LCDs

Hiroyuki OSHIMA and Shinji MOROZUMI

SEIKO EPSON Corporation
Owa 3-3-5, Suwa, Nagano, 392 Japan

The current status and future possibilities of poly-Si TFTs will be discussed, focussing on their LCD applications. From the view point of LCD trends, the future requirements for poly-Si TFTs are summarized as (1) shrinkage of design rules, (2) CMOS configuration for integrated driver TFTs and self-aligned structure for both pixel and driver TFTs, (3) lower OFF current for pixel TFTs, (4) higher mobility (higher ON current) for driver TFTs, and (5) higher aperture ratio. The technical approaches to meet the requirements are presented for low temperature (<600°C) processed poly-Si TFTs.

1. Introduction

Poly-Si TFT-LCDs were announced in 1983 for the application to full-color pocket TVs and were commercialized in 1984 as the world's first. Taking advantage of high mobility, self-aligned structure and CMOS configuration, poly-Si TFTs have been progressing for use in active matrix LCDs with integrated drivers.

The present paper, focussing on low temperature processed poly-Si TFTs, reveals the approaches to high performance poly-Si TFTs which will meet the future requirements based on LCD trends, and shows that poly-Si TFTs will be promising devices for high resolution and high pixel density applications such as HDTV light valves.

2. Trends for Poly-Si TFT-LCDs

Fig. 1 and Fig. 2 show the latest trends for TFT-LCDs which have developed during the past several years. In Fig. 1, the relationship between display area (size) and resolution is plotted. The resolution has been defined as the number of dots which can be operated independently. This figure shows that poly-Si TFTs have been applied to smaller and higher resolution LCDs while amorphous Si (a-Si) TFTs are aiming at larger displays such as 10" PC LCDs. Fig. 2 presents the trend between pixel area (size) and pixel aperture ratio. Poly-Si TFTs are suitable for smaller pixels and higher aperture ratio. Amorphous Si TFTs with transparent storage capacitors consisting of an insulating layer between double ITO layers are
capable of the same trend in aperture ratio as that of poly-Si TFTs, but are severely limited by defects and low yield. The aperture ratio depends on many factors, such as design rules, fabrication processes and device structure. In general, however, for a given pixel size, poly-Si TFTs will have a larger aperture ratio than a-Si TFTs.

Poly-Si TFTs will be applied to LCDs with smaller pixels, higher resolution, and higher aperture ratio. These applications with a small pixel pitch will especially require integrated drivers because of the difficulty in mounting external driver LSIs.

3. Future Requirements for poly-Si TFT-LCDs

Considering the poly-Si TFT-LCD trends described above, an example of the specifications for future poly-Si TFT-LCDs might be assumed as follows:

- **LCD Size**: 3" diagonal
- **Pixel Number**: 1920(H) x 1080(V)
- **Pixel Size**: 35 μm square
- **Aspect Ratio**: 16:9
- **Aperture Ratio**: > 50%
- **LC Capacitance**: 13 fF per pixel

The application of such LCDs will be light valves for HDTV LCD projectors, which is one of the important targets for poly-Si TFT-LCDs.

In order to realize future LCDs, high performance TFTs with specifications such as those given below will be required.

- **Mobility**
  - for Pixel: > 5 cm²/V·sec
  - for Driver: > 100 cm²/V·sec
- **OFF Current**
  - for Pixel: < 0.1 pA
  - for Driver: < 1 nA
- **TFT Polarity**
  - for Pixel: either Nch or Pch
  - for Driver: both Nch and Pch (CMOS)
- **TFT Parasitic Capacitance**: < 1 fF

Since the cost of 3" LCDs incorporating high temperature processed (HTP) poly-Si TFTs on small quartz substrates will no longer be competitive, low temperature processed (LTP) poly-Si TFTs on large glass substrates will be essential to meet the above requirements. Therefore, the following discussion will concentrate on LTP poly-Si TFTs.

A major subject in LTP poly-Si TFTs is control of the MOS interface by methods other than the thermal oxidation of the gate insulator used in HTP TFTs. ECR-CVD SiO₂ is a promising solution to this problem. The application of ECR-CVD to actual TFT-LCDs will be presented in the following poster session.

4. Approaches to High Performance Poly-Si TFTs to Meet Future Requirements

The approaches to satisfy the future requirements in LTP poly-Si TFTs can be summarized as follows.

(1) **Shrinkage of Design Rules**

Decreased design rules and miniaturized poly-Si TFTs will be quite important to achieve higher aperture ratio and smaller parasitic capacitance of the devices.

Smaller TFTs also provide better I-V performance such as high ON current and small OFF current as shown in Fig. 3. ON current is inversely proportional to channel length while OFF current is mainly determined by the channel-drain edge and is unaffected by channel length.

2 μm design rules will be required in the near future.

(2) **CMOS and Self-Alignment**

A CMOS configuration consisting of both Nch and Pch TFTs is indispensable for driver integration. Self-aligned TFTs provide minimum parasitic capacitance resulting in smaller storage capacitors in the pixels and high speed operation in the integrated drivers. Even if the driver circuits are not integrated, a self-aligned structure will be essential to realize higher aperture ratios.

The combination of 2 μm design rules and self-aligned structure can reduce the parasitic capacitance to less than 1 fF.

The key technology for CMOS and self-aligned processes will be Ion-Doping, which is suitable for large area doping in contrast to conventional Ion-Implantation.

(3) **Lower OFF Current**

Poly-Si TFTs have suffered from relatively high OFF current compared with a-Si...
TFTs. This is a serious problem for pixel TFTs since the fundamental principle of active matrix displays is based on static operation without leakage current.

Fig. 4 shows a useful suggestion for solving the OFF current problem. Adopting an "On-The-Line" structure between the gate edge and the drain edge (Fig. 4(a)), the OFF current can be drastically reduced as shown in Fig. 4(b). Considering the principal cause of the OFF current, a LDD or offset structure near the drain region can be effective in reducing the OFF current. The target OFF current of less than 0.1 pA will be successfully achieved using such kinds of technology.

If the OFF current in the dark condition can be sufficiently reduced, poly-Si TFTs will be suitable devices for LCDs since poly-Si TFTs, in contrast to a-Si TFTs, are insensitive to incident light and have little photo-current.

(4) Higher Mobility (Higher ON Current)

Although the poly-Si TFT mobility of around 5~10 cm²/V·sec is sufficient for pixel transistors, drastic enhancement in mobility will be required for driver integration.

![TFT structure diagram](image)

(a) TFT structure

![TFT characteristics graph](image)

(b) TFT Characteristics

Table 4 Effect of gate-drain overlap on OFF current.

<table>
<thead>
<tr>
<th>MOBILITIES(cm²/V·sec)</th>
<th>Nch</th>
<th>Pch</th>
</tr>
</thead>
<tbody>
<tr>
<td>(L=10 μm)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>as-deposited poly-Si</td>
<td>6</td>
<td>3</td>
</tr>
<tr>
<td>SPC</td>
<td>25</td>
<td>18</td>
</tr>
<tr>
<td>Laser Annealing</td>
<td>187</td>
<td>60</td>
</tr>
</tbody>
</table>

Table 1. Comparison of mobilities in Nch and Pch TFTs among three techniques.

Three approaches to mobility enhancement are compared in Table 1. The effort to optimize as-deposited poly-Si films is important since it is the most fundamental and simplest way to improve the mobility and is suitable for LCDs without integrated drivers. SPC (Solid Phase Crystallization) is carried out under thermal equilibrium conditions and is easily applied to large area substrates with high uniformity. Laser annealing results in drastic mobility enhancement and can reach the target specification of more than 100 cm²/V·sec for driver integration, but it is still a little premature for practical use. The details of these three approaches will be described at the poster session.

(5) Higher Aperture Ratio

While shrinkage of design rules, self-aligned structure and lower OFF current contribute to the enlargement of aperture ratio, further improvement will be necessary for 35 μm square pixels to keep brighter displays. For example, incorporation of the black matrix onto the TFT substrate and/or shrinkage of the liquid crystal cell gap without sacrificing the optical characteristics may be candidates for achieving higher aperture ratio.

5. Summary

The approaches to high performance poly-Si TFTs which will meet the future requirements dictated by LCD trends have been presented. By combining these technologies, poly-Si TFTs will be promising devices for high resolution LCD applications.

6. References

1) S. Morozumi, H. Ohshima et al., SID'83 Digest, 158 (1983)
2) H. Ohshima and S. Morozumi, IEDM'89 Digest, 157 (1989)
3) S. Morozumi, H. Ohshima et al., SID'84 Digest, 316 (1984)
4) G.Kawachi et al., SSDM'90 Extended Abstract, 971 (1990)
5) K. Masumo et al., ibid, 975 (1990)
6) Y.Hayashi et al., Eurodisplay'90 Proceedings, 60 (1990)