#### Invited

# HF and UV-Ozone Integrated Wafer Preclean: Chemistry and Effects on Thermal Gate Oxide

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Monolayer amounts of contaminants or surface residues after silicon surface cleaning are shown to have significant impact on the electrical integrity of simple test device structures. Si surfaces are exposed to controlled amounts of various chemical species, such as hydrocarbons, oxide, hydrogen, or fluorine, using an integrated processing system with in-situ analysis capability. Thermal oxides are grown in-situ on those surfaces and poly or metal-gate capacitors are fabricated. Some surface species, such as carbon, are found to be detrimental to the oxide quality after processing, whereas others enhance it's properties, e.g., fluorine. Process integration sometimes enhances device sensitivity to molecular contaminants because these species are preserved throughout processing.

#### INTRODUCTION

Improved control of surface contamination is mandatory to achieve the defect densities forcasted for future ULSI generations1. Traditionally, only particles have been recognized as a critical surface contamination and have attracted significant at-However, molecular surface contamtention. ination will also have important consequences for device performance and reliability as device dimensions shrink and process temperatures de-This requires an understanding of the crease<sup>2</sup>. reactivity of different chemical species and reaction pathways of surface contamination during processing in order to develop schemes that effectively remove or prevent such contamination. Furthermore, any correlation between such molecular contamination and degradation in the electrical properties of the resulting device structure needs examination. Lastly, the advent of integrated processing adds an additional degree of complex-In the absence of atmospheric conditions, ity. species left at the surface remain there unaltered and can affect the reactivity during a subsequent process, thereby introducing an new degree of process interaction.

## EXPERIMENT

The integration of surface cleaning with analysis in an integrated processing equipment<sup>3</sup> without air exposure between the two steps allows unambiguous characterization of the as-cleaned surfaces, and a correlation with electrical figures of merit of simple, in-situ processed device structures (MOS/poly-gate capacitors). 3.25" diam. Si(100) wafers have been prepared using different methods: (a) RCA clean as control, (b) diluted HF dip clean, (c) UV-ozone clean, and (d) controlled contamination of HF-cleaned surfaces under inert atmosphere with selected, pure hydrocarbons. As cleaned wafers were loaded under inert, highly purified atmosphere, pumped to ultrahigh vacuum (UHV) conditions, and the state of the surface was analyzed using techniques such as X-rav photoemission spectroscopy (XPS). Wafers were also loaded under UHV conditions into the UHV-compatible oxidation reactor (base pressure 10-8 torr) where they were ramped up to temperature after the reactor had been vented with either ultra-pure Ar or oxygen. Thermal oxidation was performed at 850°C to grow  $\simeq 12 \text{ nm SiO}_2$ . After oxidation, the metal electrode was fabricated exsitu.

# **RESULTS AND DISCUSSION**

HF treated wafers were found to be essentially free of oxide and hydrocarbon contamination, but terminated with a layer of adsorbed hydrogen<sup>4</sup> as evidenced by high resolution electron energy loss spectroscopy (HREELS) in Figure 1 (lower trace). This surface is comparatively stable in ambient air against re-oxidation<sup>5</sup>. A small amount of fluorine was detected by XPS and identified as Si-F species. The hydrogen-terminated surface was found to be very susceptible to contamination with hydrocarbons<sup>6</sup>. Thermal desorption spectroscopy (TDS) indicates that the hydrogen passivation after HF exposure is removed from the wafer surface after anneal to  $\simeq 500^{\circ}$ C, leaving the Si surface exposed. Hydrocarbons present at the surface dur-



Figure 1: High resolution electron energy loss spectra for a clean, freshly IIF dip-cleaned Si(100) wafer compared with a heavily hydrocarbon contaminated sample after UHV anneal to 700°C for 10 minutes. Changes in the total hydrogen coverage bring about changes in the SiH vibrational spectrum. Formation of SiC is seen.

ing such an anneal react to form Si-C species (seen in the upper trace of Fig. 1). Upon further anneal, sufficient amounts of Si-C species will result in the formation of SiC aggregates. The presence of significant amounts of Si-C species at the Si-SiO<sub>2</sub> interface severly degrades the integrity of a gate oxide. Figure 2 shows how a valeric acid contamination of  $\simeq 1$  monolayer present prior to oxidation can impact the breakdown field strength, interface state density and fixed charge density of a 120Å thick gate oxide<sup>6</sup>. It is obvious that such contamination cannot be tolerated.

By contrast, UV-ozone treated or RCA-cleaned wafers are terminated with a thin oxide layer ( $\simeq 1$ nm thick). The UV-ozone process removes surface hydrocarbon contamination via formation of volatile CO or CO<sub>2</sub>. It furthermore enriches the oxide Si-OH species produced during laver with oxidation of the surface hydrogen after HF clean, as well as with Si-OF species 7. During thermal oxidation a significant fraction of the fluorine species remain in the growing oxide. In contrast to carbon incorporation, fluorine accumulation at a UV-ozone cleaned surface seems beneficial<sup>8,9</sup>. Figure 3 shows the shifts in flatband voltage and Dit upon carrier injection for three MOS devices with different amounts of incorporated fluorine. Apparently, the presence of Si-OF species in the oxide and near the Si-SiO2 interface stabilizes the oxide against hot-carrier and radiation damage effects10.



Figure 2: Electrical evaluation of Al-gate MOS capacitors fabricated on 12 nm thermal oxides grown on RCA cleaned and (HF + valeric acid) treated sample surfaces. The figure plots (left) breakdown field strengths and (right) highfrequency quasi-static CV curves for the two samples. Note the high  $D_{it}$  value (cm<sup>-2</sup> eV<sup>-1</sup>) and the large negative shift in the flat-band voltage for the contaminated sample.



Figure 3: Plot of the flat-band voltage and  $D_{it}$  as a function of the Fowler-Nordheim injected current fluence. Constant current stress by injection from the gate was carried out for periods of 10 secs. The oxide field was 6-7 MV/cm.

Even in the absence of potential contaminants such as fluorine or carbon, the difference in thermal stability of surface hydrogen compared to a surface oxide can severly impact gate oxide integrity<sup>11</sup>. A breakdown statistics of wafers cleaned with the standard RCA clean is compared to breakdown statistics of wafers after initial HF and UV-ozone clean in Figure 4. It is only for ramp-up to temperatures above  $\simeq 700^{\circ}$ C in an inert ambient containing trace amounts of impurities (ppm ppb of  $H_2O$  or  $O_2$ ) that the quality of the thin oxide is significantly deteriorated. Low concentrations of  $O_2$  at elevated temperatures cause etching of the surface due to the formation of vol-The etching reaction<sup>12</sup> roughens the atile SiO. surface prior to oxidation and impacts the breakdown dehavior due to interfacial field enhancement<sup>11</sup>. Surface roughening due to etching of the bare Si surface occurs only on the HF cleaned surface because the surface passivation layer (hydrogen) desorbs in that case at temperatures well below the process temperature. In contrast, a thin oxide film will persist during an anneal to process temperatures of  $\simeq 850^{\circ}$ C thereby protecting the Si surface against the etching reaction. In ultraclean, integrated processing equipment this difference in film stability has a strong impact, because the chemical state of the surface is preserved between final cleaning and oxidation, In contrast, traditional processing, due to moisture exposure during temperature ramp-up, will lead to sufficient oxidation of an HF-cleaned surface to slow the etching reaction.

> Al/12 nm SiO<sub>2</sub>/Si 100 8-8-8-8-8-HF clean cumulative failures (z) 80 60 40 20 RCA clean -O3 clean AAAAAA 0 4 8 0 12 16 20 FIELD (MV/cm)

Figure 4: Cumulative breakdown statistics for integrated precleaned and thermally oxidized samples. The different treatments are HF dip, RCA clean, and a vapor phase  $UV/O_2$  clean.

## CONCLUSIONS

In this brief review of results published in detail elsewhere we have demonstrated clearly that the state of the surface after a cleaning step can have profound consequences for the quality of a subsequently grown oxide layer. Foreign chemical species present at the surface in quantities of a monolayer or less  $(10^{14} - 10^{15} \text{cm}^{-2})$  are seen to impact the figures of merit of gate oxides such as trap state density, breakdown field, and radiation sensitivity. These effects could be correlated to the formation of SiC, SiOF, or SiO species during processing. It is obvious that similar relations can be established for processes other than thermal oxidation, such as, e.g., silicon epitaxial growth. Establishing correlations between detailed process chemistry and resulting device parameters is essential to understand, predict and control molecular contamination in future device generations.

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