Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials, Yokohama, 1991, pp. 496-498

Invited

New Techniques in Vapor Phase Wafer Cleaning

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A novel vapor phase cleaning system employing a single wafer, silicon carbide process chamber is described. The use of heat and ozone for organic contamination removal provides improved uniformity of subsequent oxide etching. Data are presented which demonstrate selective removal of native oxide in HF/H_2O vapor. A comparison of vapor phase and aqueous pre-gate oxide cleans indicate greatly improved oxide integrity for vapor cleaned structures.

1. INTRODUCTION/BACKGROUND

Since the 1950's, wafer cleaning processes have been a critical part of the device fabrication sequence. In general, these cleans have been carried out using aqueous solutions, based in part on those processes developed by Kern (1). However, as device geometries have decreased below one micrometer, increased problems have arisen due to the inadequacies of liquid-type cleaning.

On the other hand, vapor phase cleaning and etching of silicon wafers have demonstrated many advantages. These include improvements in technical capabilities (better control with smaller geometries) as well as environmental aspects (reduced chemical usage and disposal) (See for instance Ref 2-4). In addition, vapor cleaning is much more compatible with cluster-type integrated processing (5). In this paper, a new vapor phase wafer cleaning system and associated processes are described. Examples of uniform oxide etching and selective native oxide removal are presented, along with a key device application - that of pre-gate oxidation cleaning. The value of vapor phase cleaning is demonstrated in this latter case by a comparison of oxide electrical properties - especially integrity - between vapor and liquid pre-oxide cleaning treatments.

2. SYSTEM AND PROCESS

A schematic of the recently developed vapor phase cleaning system is shown in Fig. 1 (6). Hydrofluoric acid and/or water vapor is delivered to the reaction chamber from heated vaporizers (VAP 1 and VAP 2) using selected carrier gases (N_2, Ar, or

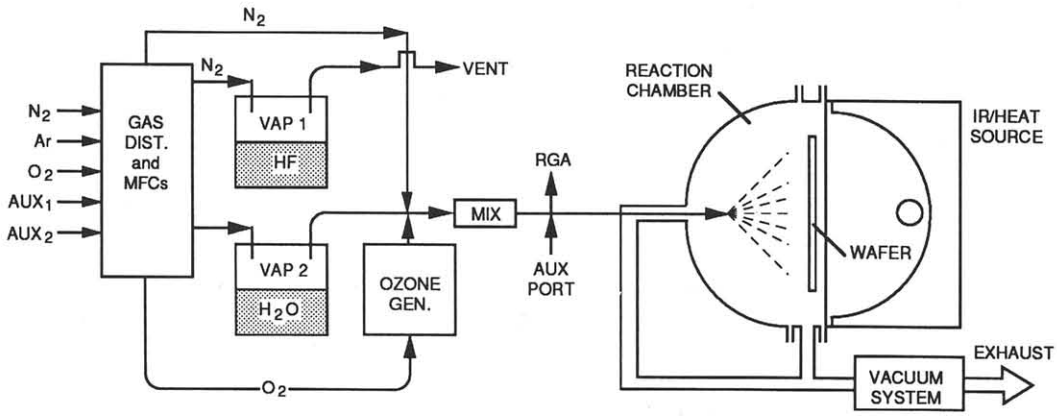

Fig. 1. Schematic of vapor phase wafer cleaning system.

O_2). The silicon carbide reaction chamber, maintained at constant temperature, is typically evacuated before and after a cleaning cycle, which is generally carried out at reduced pressure (100-400 Torr). Reaction time varies from 5-60 seconds, depending on the process. Gas flow rates are 5-15 liters/min and are controlled by mass flow controllers, along with suitable solenoid valves (not shown). Unlike previous versions of this system (6), the wafer can be heated up to 400°C by an infrared heat source. In addition, ozone can be added to the vapor reactants.

Concentrations of HF and H_2O, which condense on the wafer surface, can be varied by controlling temperatures of the two vaporizers and carrier flow rates through the vaporizers. In addition, other reactant gases, such as HCl or alcohols, can be employed for particular applications. Organic contamination can be removed from the wafer surface prior to the clean/etch step by heating the wafer to 200°C or above in ozone, and cooling back down rapidly to below 20°C, where etching occurs. Wafers up to 200 mm are processed individually in one to two minutes using computer controlled, automated wafer handling.

3. UNIFORM OXIDE ETCHING

One of the applications of vapor phase cleaning is the removal of oxide films - either partially or back to the silicon substrate. In either case, it is very important that this etch-back be as uniform as possible. Such a process may be evaluated for both uniformity and repeatability by mapping oxide thickness before and after etching, using a thickness monitor such as the Prometrix Surfscan or an ellipsometer. Plots of oxide thickness versus etch time are used for the evaluation. Because of the condensation mechanism associated with this process (7), delay or offset times may be observed before etching begins, depending on process conditions and oxide surface characteristics. The etching itself is usually linear with time in the range 1-50Å/sec.

It has been determined that various types of impurities, such as hydrocarbons, may deposit on the oxide surface from the ambient, and severely affect etch uniformity. Thus, it was determined that a ozone pre-treatment at 200°C or above prior to the etching would remove this impurity and etch uniformity would greatly improve. The following experiment describes the effectiveness of this heat/ozone pre-oxide etch treatment. Twenty-five 150 mm wafers were removed from a box and approximately 500Å of oxide vapor etched. Prior to the etching, every other wafer was given a heat/O_3 pretreatment. Results were as follows:

No Pretreat:	Ave. 1 sigma uniformity = 6.17% (5.08 - 7.17)
Pretreat:	Ave. 1 sigma uniformity = 2.12% (1.81 - 2.46)

Similar improvements were obtained for repeatability.

4. SELECTIVE OXIDE ETCHING

In the processing of various device structures, such as gate oxides, metal contacts, etc., it is desirable to remove chemical or native oxide from an opening in an oxidized layer, with minimum etching of the surrounding thick oxide. Such selective etching has been reported for anhydrous or very dry HF processes (8, 9). It has also been found that vapor phase selective etching of these thin layers can be achieved in HF-H_2O mixtures by taking advantage of the delay or off-set phenomena mentioned above. In Fig. 2, plots of oxide-etched versus etch-time are shown for both a 10Å native oxide and a thicker thermal oxide. Because the conditions of this particular process resulted in a 12 second delay in commencing etching of the thermal oxide, most of the native oxide could be removed (down to 3Å) without any attack of the thermal oxide.

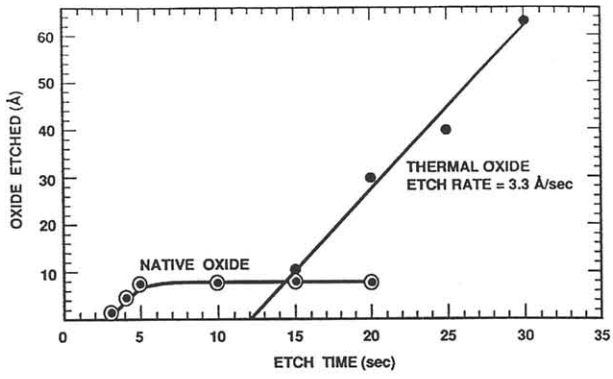

Fig. 2. Selective etching of native oxide in presence of thermal oxide using vapor phase HF process.

5. PRE-GATE OXIDE CLEAN

Several important applications which have been shown to be enhanced by vapor phase cleaning pre-treatments have been identified. These include silicide deposition, epi- and poly-Si deposition, metal-to-silicon contacts, and gate oxidation. Experiments have been carried out to determine advantages of vapor phase pre-gate oxide cleans as compared to conventional aqueous cleaning sequences. The most critical property of gate oxides relates to oxide integrity (10). A measure of this integrity includes current-voltage breakdown

characteristics, stress endurance (such as charge-to-breakdown), charge trapping, and oxide interface charge generation.

A number of process variables have been evaluated in addition to the comparison of vapor phase versus aqueous gate oxide pre-cleans. These included: with and without sacrificial oxides, furnace thermal oxide versus rapid thermal oxide, post vapor clean DI water rinse versus no rinse, and HF-H_2O versus HF-HCl-H_2O vapor cleans. Two typical results are presented in Figs. 3 and 4, where oxide electrical properties are compared for vapor phase and conventional aqueous pre-oxidation cleans. In Fig. 3, an oxide breakdown histogram is shown for a 135Å thermal oxide, where poly-Si capacitors with 0.0004 cm^2 were used. Breakdown fields of 12.7 MV/cm were observed for the vapor phase pre-cleans, compared with 11.9 MV/cm for aqueous pre-cleans. Charge-to-breakdown data are plotted in Fig. 4 for these same oxides. Stress field

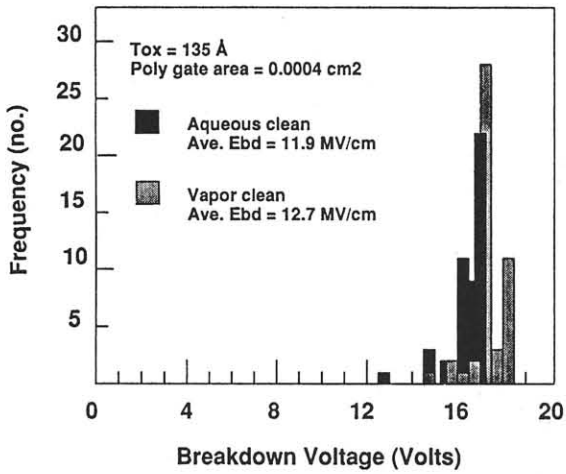

Fig. 3. Oxide breakdown histograms for vapor and aqueous pre-cleans.

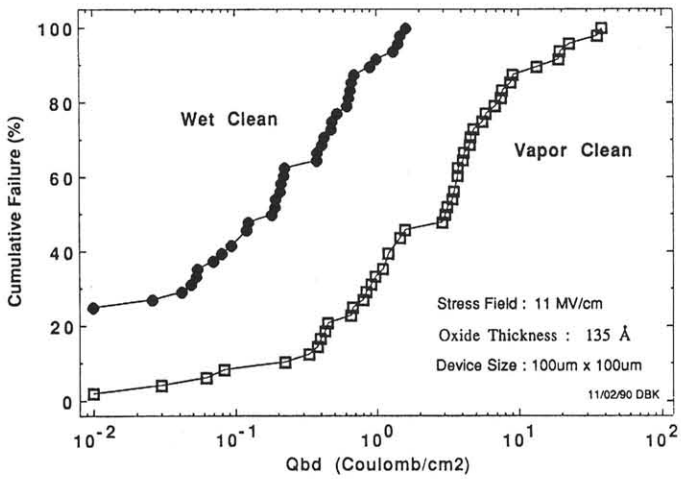

Fig. 4. Charge-to-breakdown (Q_{bd}) plots for thermal oxides with vapor and aqueous pre-cleans.

was 11 MV/cm and device size was 100 x 100 μm. Again, it can be observed that the vapor phase results were significantly better than those of aqueous pre-cleans.

6. SUMMARY

A novel vapor phase cleaning and oxide etching system, based on HF and related chemistries, has been described. This system, which employs a single wafer, silicon carbide process chamber, also employs heat and ozone for removing organics prior to oxide etching or cleaning; preliminary data are presented which show improved oxide etch uniformity. Also discussed are experiments which indicate that selective removal of thin native or chemical oxides can be achieved, even in the presence of water vapor. Finally, a comparison of various electrical properties of MOS-type gate oxides indicates that vapor phase pre-gate oxide cleaning provides significantly improved results compared to conventional aqueous cleans. It may also be noted that in addition to using much less chemicals, vapor phase cleaning is readily adaptable to cluster-type integrated processing.

7. REFERENCES

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