

## High Performance Copper Metallization for ULSI Interconnects

Masahito OTSUKI, Toshiyuki TAKEWAKI, Hideshi KUWABARA,  
Tadashi SHIBATA, Tadahiro OHMI and Takahisa NITTA\*  
Department of Electronics, Tohoku University, Sendai 980 Japan  
\*) Device Development Center, Hitachi Ltd., Ohme, Tokyo.

### Abstract

High quality low-resistivity Cu thin films have been successfully formed by low-kinetic energy particle bombardment process. The Cu films have exhibited three to five orders of magnitude larger electromigration lifetime than that of Al-Si based alloy interconnects. Moreover, very low contact resistance of  $3 \times 10^{-7} \Omega \text{ cm}^2$  for Cu/n<sup>+</sup>-Si contacts as well as ideal Schottky diode characteristics for both Cu/n-Si and Cu/p-Si contacts have been demonstrated.

### Introduction

The enhancement in the integration density and speed performance of ULSI circuits requires the miniaturization of transistors and interconnects as well as higher current driving capabilities for transistors. As a result, large currents must be conducted through long interconnects having small cross sections and through small contacts. Therefore a new metallization scheme which ensures high electromigration reliability as well as low bulk resistivity and low contact resistances must be established.

Aluminum is the major material used for interconnects in integrated circuits. However its resistivities is not low enough to operate ULSI circuits at ultra-high speed. Furthermore, aluminum is liable to show poor reliability against failures caused by electromigration and stress-migration. Copper (Cu) is now drawing considerable attention as an alternative to Al due to its low bulk resistivity ( $1.72 \mu \Omega \text{ cm}$ ) and large electromigration resistance[1-3].

The purpose of this paper is to present a high performance copper metallization realized by low-kinetic energy particle bombardment process[1,4]. High quality low-resistivity Cu thin films have been successfully formed by the process, which have exhibited three to five orders of magnitude larger electromigration lifetime than that of Al-Si based alloy interconnects. Moreover, very low contact resistance of  $3 \times 10^{-7} \Omega \text{ cm}^2$  for Cu/n<sup>+</sup>-Si contacts as well as ideal Schottky diode characteristics for both

Cu/n-Si and Cu/p-Si contacts have been demonstrated.

### Experimental

The substrates used were n-type (100) Si wafers on which 1000Å thermal oxide films were grown. In order to supply a dc substrate bias voltage to a metal film grown on SiO<sub>2</sub>, the SiO<sub>2</sub> film was partially etched off. Substrate dc bias is varied from +10V to -80V, and about 1.0 μm thick Cu films were grown. After Cu deposition, thermal annealing was carried out at various temperatures of 140 °C-600 °C in argon or nitrogen ambient.

The crystal structures of Cu films before and after thermal annealing were investigated by X-ray diffraction analysis and reflection electron diffraction analysis, and the surface morphology was evaluated by using scanning electron microscope (SEM). The Cu film resistivities were measured by the Van der Paw method. And electromigration test was carried out using newly developed accelerated life-test method[5]. For fabricating Schottky diodes, window patterns of 40 μm x 40 μm ~ 2mm x 2mm were opened in thermal oxides grown on n- and p-type silicon wafers, and Cu film were deposited by employing N<sub>2</sub>-gas seal native-oxide-free processing[6], and then delineated into electrode patterns.

## Results and Discussion

Figure 1 shows the orientation of Cu films after post-metallization anneal as a function of the annealing temperature and the substrate bias voltage applied during the film growth. As deposited films exhibit (111) orientation regardless of the ion bombardment energy. However, the film undergoes almost perfect transformation from (111) to (100) orientation when relatively high ion bombardment energies ( $V_s < -50V$ ) are employed for film growth. Such transformation is always accompanied by large grain growth in the Cu film, which has been confirmed by the surface morphology observation and reflection electron diffraction analysis. In Fig.2 is shown the temperature dependence of Cu thin film resistivity before and after the thermal anneal at 450 °C. The film after anneal exhibits a room temperature resistivity of  $1.78 \mu\Omega\text{cm}$ , almost identical to the bulk value. One order of magnitude reduction in the residual resistivity is also observed. These results are the direct consequence of the large grain growth that occurred in the film. The results of electromigration test carried out on Cu interconnects using newly developed accelerated life-test method[5] are shown in Fig.3 along with the data for Al-Si interconnects, demonstrating the large electromigration resistance of the Cu interconnects. When the data are extrapolated to a room temperature (300K), Cu interconnects after thermal anneal have values of  $\tau J^2$  which is approximately five or three orders of magnitude larger than that for the Al-Si or Al-Cu-Si interconnects studied here, respectively.

Figure 4 shows the Schottky barrier heights for Cu/n-Si contacts for four different contact areas. The fluctuation of  $\phi_{bn}$  is less than 0.005eV, and the value is independent of the contact area over four orders of magnitude.

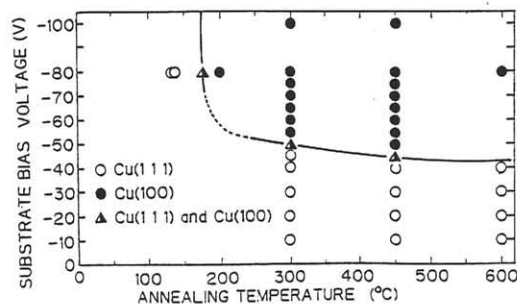


Fig.1 Crystal orientation of Cu films after post metallization anneal for 30 min. as a function of temperature and the DC wafer bias voltage applied during film growth.

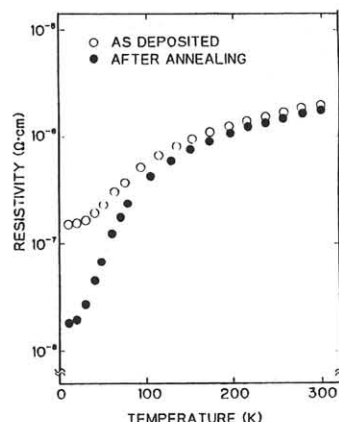


Fig.2 Temperature dependence of Cu thin film resistivity before and after thermal anneal at 450 °C.

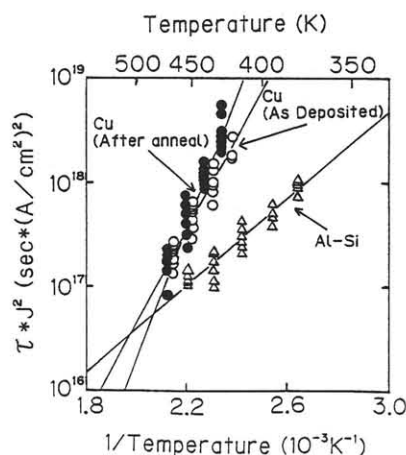


Fig.3 Arrhenius plot of  $\tau J^2$  ( $\tau$ :electromigration lifetime,  $J$ : stress current density ) for Cu and Al-Si interconnects.

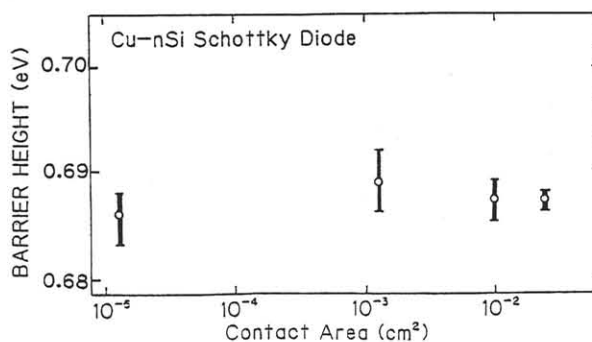


Fig.4 Barrier heights of Cu/n-Si Schottky diodes as a function of contact area.

Figures 5(a) and (b) show the temperature dependence of saturation current density for as deposited(non-alloyed) Cu/n-Si and Cu/p-Si Schottky contacts, respectively. The Schottky barrier heights determined from the slope of these lines are 0.707eV and 0.469eV for n-Si and p-Si, respectively, and their sum 1.176eV is almost the same as the value of Si bandgap, demonstrating the formation of ideal Cu/Si contacts. And the Cu/n<sup>+</sup>-Si contact resistance as low as  $3 \times 10^{-7} \Omega \text{ cm}^2$  has been also achieved without any alloying heat cycles.

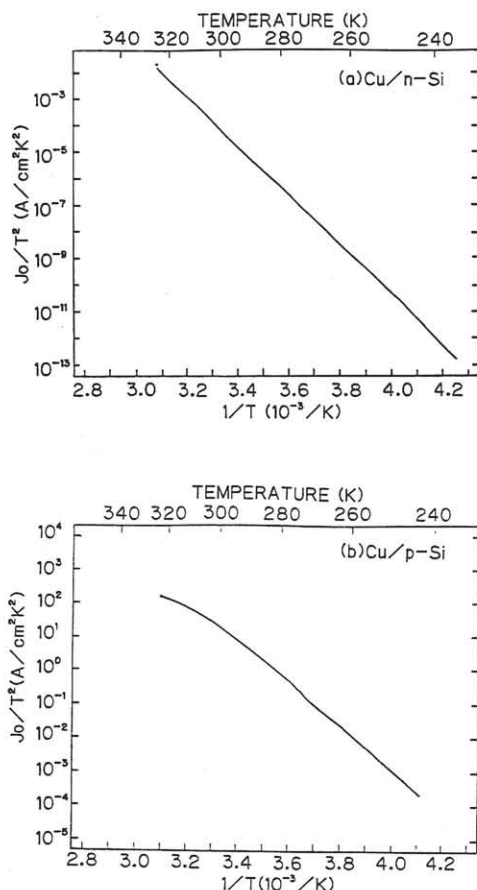


Fig.5 Temperature dependence of Saturation current density for non-alloyed Cu/n-Si(a) and Cu/p-Si(b) contacts.

## Conclusions

High performance Cu metallization has been developed by a low-kinetic energy particle process. Completely (100) oriented Cu films having grains as large as  $100 \mu\text{m}$  are obtained by depositing Cu films on  $\text{SiO}_2$  followed by thermal annealing. The residual resistivity of Cu films after thermal annealing is approximately one order of magnitude lower than that of non-thermal annealed Cu films.

Furthermore, Cu interconnects after thermal anneal have exhibited three to five orders of magnitude larger electromigration lifetime than that of Al-Si based alloy interconnects. Moreover, formation of ideal Schottky diode characteristics as well as very low contact resistance of  $3 \times 10^{-7} \Omega \text{ cm}^2$  without any alloying heat cycles have been demonstrated.

High performance Cu metallization developed in this work featuring high electromigration resistance as well as low bulk resistivity and low contact resistance is quite promising to use in future ULSI devices.

## REFERENCES

- [1] T.Ohmi, T.Saito, T.Shibata, and T.Nitta, Appl. Phys. Lett. 52, 2236(1988).
- [2] N.Awaya and Y.Arita, Dig. Tech. Papers, 1989 Symp. VLSI Technology, Kyoto, P.103.
- [3] J.S.H.Cho, H-K.Kang, M.A.Belley and S.S.Wong, Dig.Tech.Papers, 1991 Symp VLSI Technology, Oiso, P.39.
- [4] T.Ohmi, T.Saito, M.Otsuki, T.Shibata, and T.Nitta, J.Electrochem.Soc., 138, 1089 (1991).
- [5] T.Hoshi, and T.Ohmi, unpublished.
- [6] M.Miyawaki, S.Yoshitake, and T.Ohmi, IEEE Electron Device Lett. 11, 448(1990).