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Invited

Ferroelectric PZT Thin Films for ULSI Memory Applications

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Ferroelectric films are attracting interest for use in non-volatile memories because of their potential advantages, including fast write times, high density, radiation resistance, and low voltage operation. These films also have a potential use in 256M and higher density memories where the storage capacitor approach becomes difficult to use. In this paper we will review the electrical requirements for gigabit level memories and explore what these requirements imply for the material properties of ferroelectric thin films. Finally, progress toward those material properties will be discussed.

1. Introduction

Memory circuits using ferroelectric thin films have been demonstrated.[1] At present these circuits are of low density but they show the feasibility of the technology. This paper will discuss the potential of this approach to ULSI or Gigascale dimensions. We will see that near the 1 Gigabit level ferroelectric non-volatile memory may be the preferred choice. The paper is organized as follows. Section 2 will cover the advantages of ferroelectric memories in general and emphasize those elements particularly important for high density memory. In section 3 we will list the performance features that can be expected from circuits at the gigabit level of integration. These features will be used in section 4 to determine the requirements which that performance places on the ferroelectric thin films. Finally, in section 5 we will discuss the progress toward those thin film properties.

2. Ferroelectric Memory Advantages

The displacement of the ion at the center of a ferroelectric unit cell provides a natural memory. It is stably located in either the top or bottom half of the cell and can be moved from one side to the other by the application of an electric field. The state of a unit cell is further stabilized by the collective nature of the material, i.e. domains of oriented cells are formed. For sufficiently large domains the energy necessary to flip the entire domain greatly exceeds the available thermal energy and the domain is stable. This mechanism leads directly to the advantages these materials have when used as a memory element.

We divide the advantages into three categories; circuit performance and design issues, reliability issues and manufacturing issues.

Ferroelectric circuits are fast, dense, and can operate at low voltages. The speed of the switching has been calculated[2] to be < 0.5 ns. Our measurements which are limited by our current circuits show it to be faster than 3 ns. The memory cell can be scaled down in size as it is similar to a DRAM cell consisting of one transistor and one capacitor which can be stacked above the transistor. This structural similarity should allow the density of ferroelectric circuits to evolve rapidly until it catches leading edge processing. Switching at less than 2 volts has been demonstrated on 1000Å films[3]. This will allow operation in the planned 3.3 or 2.0 volt supply voltage circuits without special high voltage transistors.

Reliability defines the limits of performance of the ferroelectric as with any technology. It has been demonstrated that a ferroelectric film can be switched 1e12 times and have only a 20% reduction in remanent polarization (Figure 1). Soft errors from alpha particles are a major factor limiting the reduction of the size of the storage capacitor in

proposed high density DRAMs[4]. Since the charge in the ferroelectric cell is stored as ionic displacements throughout the bulk it is practically immune to charge loss from alpha particle hits and there is no free charge to leak away. This allows reduction in cell size without reduction in data reliability.

The ferroelectric process is being developed as a module on an existing CMOS process. It is a backend process in that the transistors are completely formed before any of the ferroelectric module steps. This allows the process to be integrated with a range of technologies including CMOS, BiCMOS, GaAs, etc. etc. It is potentially a low cost process requiring 1-3 additional masks beyond the core process.

3. Gigascale Circuit Performance

Several reviews of extrapolations of technology for 256M DRAMs and beyond can be found in the literature.[4,5] Some selected features are shown in Table 1.

	64M	256M	1G
Cell size (μm2)	1.3	0.52	0.23
Vcc (V)	3.3	3.3	2.0
Sense Amplifier sensitivity (mV)	75	50	30
Minimum feature size (μm)	0.4	0.3	0.2

Table 1

We will assume those processes necessary to manufacture the non-ferroelectric portion of the circuits will have been developed by others and is not considered here.

4. Conditions on Ferroelectric Films

From the above conditions we can estimate requirements on the ferroelectric films. Figure 2 shows the relation between the minimum charge detectable by the sense amplifier, the remanent polarization, and the area of the ferroelectric capacitor. For a cell size of 0.25 μm2 the ratio of capacitor area to cell size (Afe/Ac) is approximately 1 and at a sensitivity of 30 fC, 12 μC/cm2 is needed.

For an operating voltage of 2 volts we will assume 1 volt can be used to write the memory. This requires film on the order of 1000Å thickness to acheive the same field as is used in current designs.

A 1 Gigabit chip with a 0.25 μm2 capacitor will have a total ferroelectric area of 1.0 cm2.

5. Ferroelectric Development Needed

Current ferroelectric memories are made with Lead Zirconate Titanate (PZT) films which we will use as a basis for this evaluation. These films have been deposited by sol-gel or sputtering processes. Neither process could be used to achieve Afe/Ac ≥ 1. A more conformal process is needed. Work is only just beginning on CVD based processes for PZT deposition. A target defect density for such a unit process would be ≤ .1/cm2.

To date dry patterning of PZT involves a considerable sputtering component. Greater control will be needed for the three-dimensional structures envisioned.

Tests on presently used materials demonstrate that after 1e12 cycles the remanent polarization can nearly 6 μC/cm2[6]. Without improvement in polarization an area ratio of > 2.0 would.be the get get sufficient charge for the sense amplifier. Any improvement in polarization will reduce this ratio and the reduce the difficulty of the three-dimensional structure. At 0.25-.50 μm2, the capacitor area is only slightly smaller than 1 grain. (Grain size of 0.8 μm was seen from TEM[7]). A reduction in grain size may be needed in order to have multiple grains per capacitor. This would reduce the variation in capacitor properties as the properties would be determined by an average over grains and not dominated by a single grain.

Retention of data limits the reliability of the current generation of non-volatile ferroelectric memories. This is not a limitation for a DRAM based on the non-volatile design. The retention goal for non-volatile operation is 10 years.

It is feasible that capacitor storage can be replaced with ferroelectric storage at gigabit levels. Current material properties are within an order of magnitude of that required for such memories and development work has begun on the necessary deposition and patterning processes to manufacture such memories.

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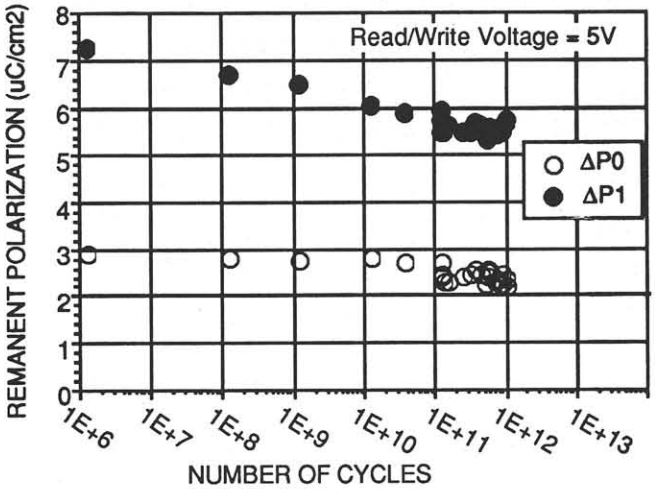

Figue 1. Fatigue of ferroelectric capacitor

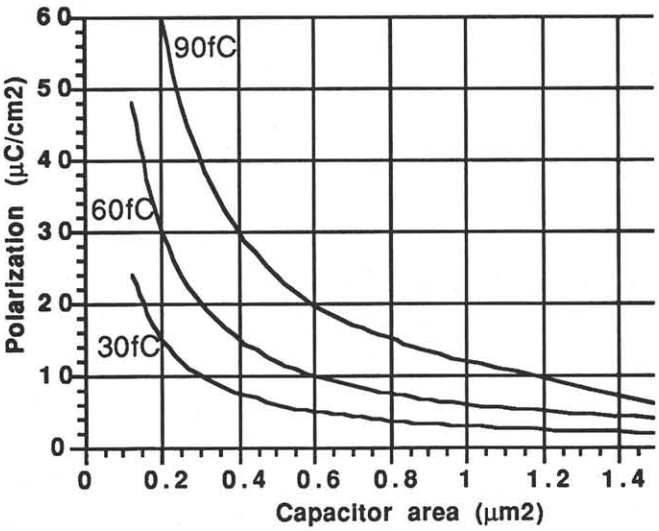

Figure 2. For sense amplifier limit graph shows polarization needed for given area.

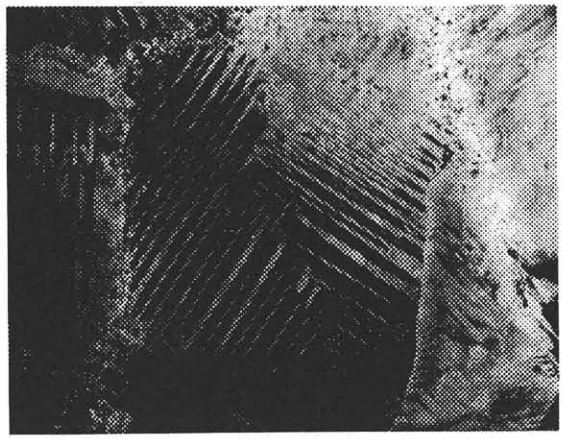

Figure 3 TEM of PZT showing domains.