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**Invited**

# A Perspective on Next Generation Silicon Devices

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Minimum size of conventional silicon devices determined by their circuit performance, the possibility of quantum-mechanical engineering of electronic properties of silicon and minimum size of silicon devices due to edge uncertainty and statistical fluctuation of dopant distribution are considered to discuss the future of silicon devices. The stress effect, Brillouin zone folding, low dimensional electron and artificial nanostructure will be useful tools for engineering of electronic properties of silicon. Breakthrough for doping technique should be exploved to overcome the minimum size limit determined by the statistical fluctuation of dopant distribution.

## 1 INTRODUCTION

Future prospect of silicon devices has been discussed in many articles, sometimes based on the so-called trend curve on shrinkage of device size. For the past three decades of years the evolution of silicon device technology coincided well with the prediction using the trend curve. The present argument is not intended to rely on the trend curve. However by simply extending the trend curve on the size of silicon devices, the shrinkage to the order of ten nanometers or below is thought to be feasible in the next generation, at least in laboratory. So far the principle of operation of existing silicon devices is semi-classical in most cases, but quantum-mechanical effects in silicon has a possibility to lead such nano- miniaturized devices to new innovation. Here after discussing the minimum size of conventional silicon devices with attention to their circuit performance, the possibility of quantum-mechanical engineering of electronic properties of silicon using stress effect, Brillouin zone folding, low dimensional electron, and artificial nanostructure will be explored. Then the edge uncertainty and statistical fluctuation of dopant distribution will be picked up as limiting factors to determine the minimum of size of silicon devices.

## 2 MINIMUM SIZE OF MOSFETS BY CIRCUIT PERFORMANCE

As a conventional type of silicon devices, which are commonly used in VLSIs, MOSFETs are chosen and their minimum size determined by circuit performance will be discussed here. Minimum size of MOSFETs was discussed by taking into account various physical phenomena such as source-drain punch-through, short channel effect, and gate-oxide breakdown,[1][2] and the subthreshold characteristic has been found to affect seriously the performance of circuits built with MOSFETs. The degradation of circuit performance by scaling-down of MOSFETs severely limits the minimum size of MOSFETs. The logic swing, normalized by the circuit voltage, of nMOS E/D inverter and CMOS inverter, where the threshold voltage and the circuit voltage are scaled down in proportion to the channel length decrese, because of the increase of the sub-threshold current at zero gate voltage due to the decrease of threshold voltage.[3] This limits the minimum channel length to $0.1\mu$m for nMOS E/D inverters. For CMOS inverters the advantage of ratioless circuits becomes explicit and the degradation of normalized logic swing allows to scale down channel length to $0.05\mu$m, but stand-by power of CMOS inverters drastically increases while the channel length approaches to $0.1\mu$m because of the increase of sub-threshold current. Effects of subthreshold current on the performance of DRAM memory cell are more serious than on that of inverters. A result of simulation, regarding to effects of various phenomena, such as source-drain punch through, short channel, hot carriers in channel, noise, soft error caused by $\alpha$ particles and retention as a function of supply voltage indicates that the short channel effect and the retention time restriction,namely leakage currents including sub-threshold current, limit the minimum channel about $0.25\mu$m.[4][5] In general dynamic MOS circuits are more vulnerable than static MOS circuits with respect to the effect of subthreshold current. Such subthreshold current can be decreased by making MOSFETs in very thin silicon layer on dielectric film. MOSFETs on SOI substrate whose top silicon layer is a few tens nanometer in thickness demonstrates improved subthreshold

characteristics.[6][7] The mechanism of the improvement is thought that the gate is effective to electrostatically shield the electric field of the drain and prevent it to affect the source potential due to the large aspect ration of the cross section of the channel region.

This is an example how circuit performance limits the minimum size of conventional silicon devices and how the barrier can be overcome by introducing new device structure. However the minimum size of the active region of conventional silicon devices will be around $0.1\mu$m and further scale-down of conventional silicon devices will not be even plausible.

# 3 QUANTUM-MECHANICAL EN-GINEERING OF ELECTRONIC PROPERTIES OF SILICON.

By lowering the lattice temperature of device, various characteristics of devices due to phonon scattering, generation and recombination of carriers and thermal distribution of carriers can be improved. The sub-threshold current characteristic is one of them and scaling-down beyond $0.1\mu$m will be possible. Besides the advantage of lattice temperature lowering, several physical effects can be used to engineer electronic properties of silicon quantum-mechanically. The followings are just illustrating examples.

## 3.1 Stress Effect on Energy Band Structure of Silicon.

Energy band structure and, in consequence, effective mass of electron and of hole change with stress and of electrons among valley changes in multi-valley band structure the distribution.

Stressing silicon crystal by the difference of thermal expansion coefficient or/and off lattice constant between the silicon film and the substrate is commonly used. Enhancement of effective electron mobility in silicon film deposited on insulator was reported[8]. Recently enhancement of hole mobility in germanium using the stress incorporated into the heterojunction between germanium and silicon-germanium alloy was also reported.[9]

## 3.2 Brillouin Zone Folding

The artificial generation of small Brillouin zone by introducing periodic potential, whose period is longer than atomic spacing, to the crystal is well-known in the superlattice science and technology. Similar principle can be used to bring the conduction band minima of the indirect transition material to $\Gamma$ point. As simple model, for instance, the conduction band minima of silicon on $< 100 >$ axis can be brought to $\Gamma$ point by making (100) oriented superlattice with a period of 5 times the lattice constant.[10] It should be notified here that such folding of Brillouin zone is just one dimensional in the space and other conduction band minima remain unchanged with respect to the energy and the position in Brillouin zone and electrons are equally distributed to those minima. In order to obtain silicon with real direct transition energy band structure, the incorporation of three dimensional potential, that is, quantum box structure into silicon crystal is required.

## 3.3 Two Dimensional Electrons

The energy band structure of two dimensional electrons is different from that for three dimensional electrons with respect to not only the dimensionality of Brillouin zone but also the energy of the conduction band minima.[11] Suppose electrons in a two dimensional potential well, whose width is of the order of several nanometers. Those electrons lose a freedom of motion perpendicular to the well surface and become two dimensional. Such potential well can be realized physically with very thin silicon film or electrically in surface inversion layer on silicon. An interesting feature can be found in a (100) oriented potential well. Conduction band minima, doubly degenerated, exist at the center of Brillouin zone and other valleys of conduction band have higher energy than the minima and exist off the center. This band structure suggests the possibility of two dimensional direct transition material. Anisotropic conductivity can be realized with (110) oriented potential well and may lead to the invention of new devices.[12]

## 3.4 One Dimensional Electrons.

In a quantum wire electrons become one dimensional, and the number of states in momentum space is only two for electrons in the ground state and expected to result high electron mobility. [13] Even one monoatomic surface roughness severely deteriorates the property of quantum wires and experimental confirmation is left to future.

## 3.5 Nanostructures in Crystal.

Nanostructure means that the size of the structure is of the order of nanometer, namely, the wavelength of electrons in crystal. Periodical array of nanostructure such as quantum wire and quantum box introduce band-gaps in the conduction band.[14] The band-gaps are expected to be usefull for suppressing optical phonon scattering of electrons and to obtain high drift velocity under high electric field.

# 4 MINIMUM SIZE DETERMINED BY STATISTICAL FLUCTUATIONS

Minimum size of semiconductor devices determined by edge uncertainty and statistical fluctuation of dopant distribution was discussed from the early stage of integrated circuit technology.[15] Here the discussions will be briefly reviewed.

## 4.1 Edge Uncertainty.

For simplicity represent a semiconductor device as a cube whose edge demension is d, and assume that

the tolerable relative deviation of the edge demension is $\epsilon$ and the standard deviation of the distribution of edge demension is $\sigma$. Then the probability that three edge demension fall the outside of the tolerance, $S_D$, is given by the following equation.

$$S_D = 1 - (\frac{2}{\sqrt{2\pi}} \int_0^{\epsilon d/\sqrt{2}\sigma} e^{-y^2} dy)^3 \qquad (1)$$

If we assume 0.5nm as $\sigma$ and $10^{-3}$ as $S_D$, d is given as a function of $\epsilon$ shown in Table 1.

Table 1:

| $\epsilon$ | 0.01 | 0.03 | 0.10 |
|---|---|---|---|
| $d_{(nm)}$ | 250 | 100 | 25 |

The deviation of device characteristics is not always in proportion to the deviation of device size. The surface roughness scattering is strongly dependent on the correlation length of surface roughness, especially when the correlation length is of the order of the de Broglie wavelength of electron. On the otherhand the transconductance of MOSFET is rather insensitive to the fluctuation of the gate length and width and determined by the averaged gate length and width and the above discussion will give rather severe limit to the minimum gate length.

### 4.2 Statistical Fluctuation of Number of Dopants.

The average distance between dopant atoms whose concentration is $10^{18}$cm$^{-3}$ is about 10 nm. In consequence when the size of the active region of a semiconductor device is scaled down to 0.1$\mu$m or below, the statistical fluctuation of the number of dopants becomes remarkable and affects device characteristics substantially. The probability that the number of dopants in a region exceeds $N_o(1 \pm \epsilon)$, where $N_o$ is the average number of dopants and $\epsilon$ is the relative tolerance of the deviation of dopant number, $S_N$, is given by the following.

$$S_N = 1 - \frac{2}{\sqrt{2\pi}} \int_0^{\epsilon N_o^{1/2}} e^{-y^2} dy \qquad (2)$$

Assuming $10^{-3}$ as $S_N$ and $10^{18}$cm$^{-3}$ as the averaged dopant concentration, $N_o$ and d are given as a function of $\epsilon$ in Table 2.

Table 2:

| $\epsilon$ | 0.01 | 0.05 | 0.10 |
|---|---|---|---|
| $N_o$ | $\sim 10^5$ | $\sim 10^4$ | $\sim 10^3$ |
| $d_{(nm)}$ | 500 | 200 | 100 |

The size quoted in Table 2 is that found in present or near future devices and the precise control of the number of dopants or of the location of dopant atoms are required to realize nano- miniaturized devices.[16]

## 5 CONCLUDING REMARKS

A perspective on next generation silicon devices to be used in digital VLSIs was presented. MOSFETs were chosen as a conventional type of devices and the minimum channel length is concluded to be about 0.1$\mu$m due to the subthreshold characteristic. Quantum-mechanical engineering of electronic properties of silicon using stress effect, Brillouin zone folding, low dimensional electrons and nanostructures, was emphasized to introduce new functions into silicon devices. Finally effects of edge uncertainty and statistical fluctuation of dopant distribution were discussed and the latter was found to give severe limit to the minimum size of silicon devices.

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