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Control of Si Solid-Phase Nucleation by Surface Steps for High Performance Thin Film Transistors

Tanemasa Asano and Kenji Makihira

Center for Microelectronic Systems,
Kyushu Institute of Technology, 680-4 Kawazu, Iizuka, Fukuoka 820

Solid-phase nucleation process of amorphous Si(a-Si) at steps formed at SiO_2 substrate surface has been investigated. Steps were formed by either isotropic or anisotropic wet chemical etching and a-Si films were deposited by vacuum evaporation. It has been found that nucleation sites can be controlled by changing the step shape and a-Si thickness. Grain growth up to about 3μm from the step edge has been observed. n-channel MOSFET's which had steps at the source/drain edge were fabricated. They showed effective electron mobility of about 200cm^2/V·s, which is approximately one order higher than that obtained from MOSFET's fabricated in Si films formed by the conventional solid phase crystallization.

1. Introduction

Recently, Si thin film transistors(TFT's) are attracting a great deal of attention because they can be applied to such devices as liquid crystal display drivers, load transistor in static random access memory cells and three dimensional integrated circuits. Required performances of TFT's for the applications include high carrier mobility and low source-to-drain leakage current. One promising approach to achieve these performances is to prepare Si films having large crystal grains. If nucleation in solid phase crystallization of amorphous Si(a-Si) is enhanced at controlled sites, uniform thin Si films having large grains will be formed. It has been reported that solid-phase nucleation of a-Si is enhanced by forming steps at insulating substrate surface.[1] In the present work we have investigated the solid-phase nucleation process of a-Si at steps formed on SiO_2 substrate surface and found that nucleation sites can be controlled by changing the step shape and a-Si thickness. It is also demonstrated that TFT's having high transconductance can be fabricated by utilizing this step controlled solid-phase crystallization.

2. Experiment

Steps of a stripe pattern were formed on SiO_2 substrate by means of following two ways: 1) Isotropical buffered-HF etching of a SiO_2 layer(200nm-thick) formed by thermal oxidation of Si(100) wafer. 2) Anisotropical etching of Si(100) wafers with a KOH : IPA : H_2O(2 : 1 : 1) solution followed by thermal oxidation. For this process, thermal SiO_2 was used as etching mask and a 20nm thick SiO_2 layer was formed by thermal oxidation after removing the mask SiO_2. The step height was set at 100nm for both types of steps.

These substrates were loaded into a vacuum chamber having a background pressure 1×10^{-7}Pa. Prior to deposition of a-Si, samples were heated at 450°C for 60min in order to clean their surface. a-Si layer was then deposited by means of electron beam evaporation. The thickness of a-Si layer ranged from 20nm to 200nm. After deposition, samples were heated *in situ* at 450°C for 60min in order to densify deposited a-Si layer. After removing the samples from the chamber, they were treated in a boiled mixture of NH_4OH : H_2O_2 : H_2O(1 : 1 : 2). Solid phase crystallization was performed at 600°C in an N_2 ambient. The observation of crystal growth was carried out with an optical microscope and a scanning electron microscope. Before observation, the surface delineation was performed on some samples by using HNO_3 : CH_3COOH : HF(50 : 50 : 1).

3. Results and Discussion

Figures 1(a) and 1(b) show cross-sectional SEM views of steps formed by the isotropical etching and

the anisotropical etching, respectively. Before observation, the samples were slightly etched in buffered-HF acid in order to enhance the contrast between each layer. The isotropically etched edge has a rather roundly shaped step, typical shape expected for isotropical etching. The anisotropically etched step have a slope inclined 55° from the surface normal.

Figure 2 shows a variation of nucleation site at steps with a-Si layer thickness. The vertical axis of this plot means the percentage of the number of nuclei appeared at the top side(hill) of the step edge. Total number of nuclei counted was about 400–800 for each plot. We can see that the nucleation site at the step depends drastically on the shape of the step. For isotropically etched steps almost all of the nucleation takes place at the bottom side of the step. On the other hand, in the case of the anisotropically etched step, nucleation takes place at the top side of the step when Si film is thicker than 80nm and it takes place at the both top and bottom sides of the step when Si film thickness was less.

In order to investigate the nucleation mechanism, we have carried out simulation of internal structure of deposited films based on the ballistic deposition model.[2] Figure 3(a) shows a simulation result obtained for a substrate having a step inclined 55° from the surface normal. Discs(circles in the figure) were deposited along the surface normal. Migration distance from the arrival point was limited to twice of the disc diameter. This means that the substrate temperature is well below the melting point of the film material. We can see from this figure that the density of disc is low at the step compared to the flat region. Figure 3(b) shows variation of disc density with thickness at upper and lower half of the step. The density is higher at the upper half when the thickness is small. But this situation changes as the thickness increases. Comparison of this simulation result and the experimental result shown in Fig. 2 suggests that the nucleation is related to the internal stress of the film which is generated due to volume change upon annealing.

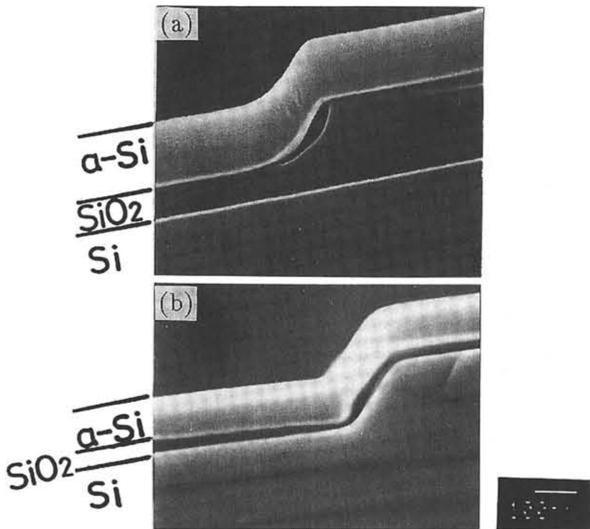


Fig. 1 Cross-sectional SEM view of the steps formed by isotropical etching(a) and anisotropical etching(b).

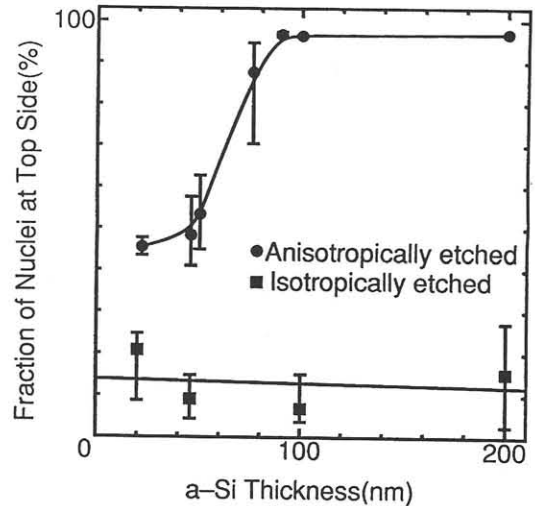
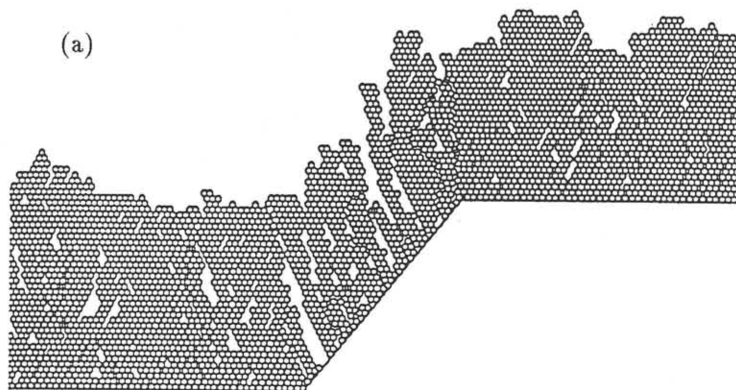


Fig. 2 Variation of nucleation site at steps with a-Si layer thickness for steps formed by isotropical etching and anisotropical etching.



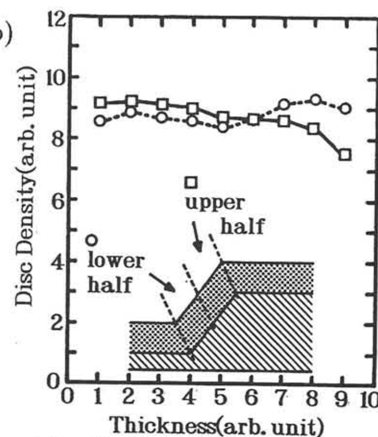


Fig. 3 (a) Internal structure of a film simulated based on the ballistic model. (b) Change in disc(circles in Fig. 3(a)) density with thickness at upper and lower half of the step.

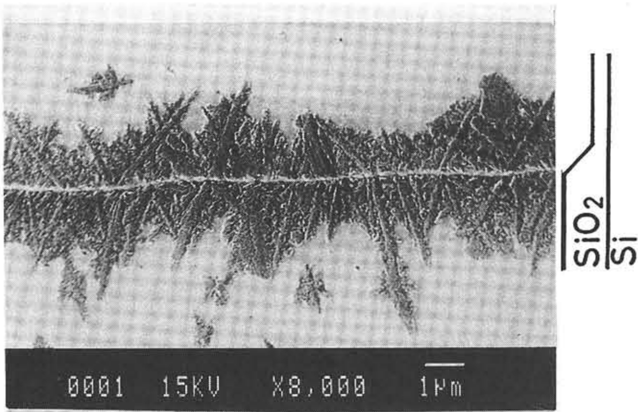


Fig. 4 SEM top view of a sample showing the grain growth from the step. the sample was annealed at 600°C for 10hours. The crystalline defects were delineated by chemical etching before observation.

Figure 4 shows a SEM top view of a sample after annealing for 10 hours. The sample surface was delineated before observation. Feature of the dendritic growth is observed. Most of the grain boundaries distributes along the normal to the step edge line. Grain growth up to about 3μm from the step edge is currently obtained.

In order to electrically characterize, n-channel MOSFET's were fabricated in Si films prepared by both nucleation controlled(stepped surface) and conventional(flat substrates) solid phase crystallization. The steps for nucleation control were formed by anisotropic etching at the source and drain edge of the MOSFET. Prior to MOSFET fabrication, post-annealing was carried out at 1100°C for 60min in an N_2 ambient. The gate oxide(100nm thick) was formed by thermal oxidation at 1050°C. Source and drain were formed by thermal diffusion at 900°C from a solid source. The thickness of the active region was set at 100nm.

Figure 5 shows typical transconductance of the TFT's. The TFT fabricated in a nucleation controlled Si film has high transconductance which is approximately one order higher than that of the TFT fabricated in a Si film formed by the conventional solid phase crystallization. The effective electron mobility of TFT in nucleation controlled Si film is about 200cm^2/V·s. This high electron mobility is owing to the size and the structure of crystal grains which is peculiar to the nucleation control by the surface step.

4. Conclusion

The nucleation site in solid phase crystallization of a-Si on SiO_2 can be controlled by changing the a-Si thickness and shape of the step. By utilizing this step-controlled nucleation, TFTs having high transconductance can be obtained.

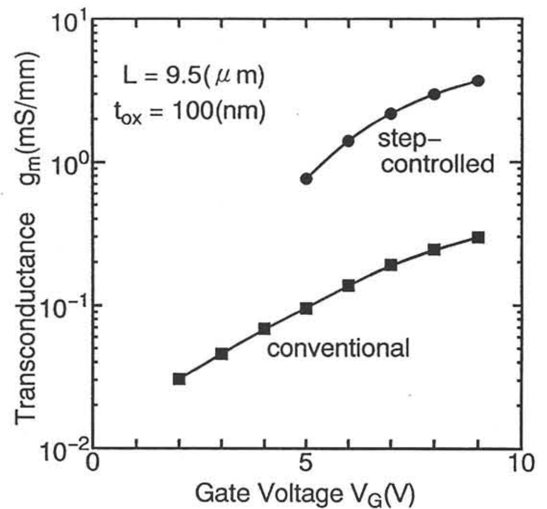


Fig. 5 Comparison of transconductance of TFT's fabricated in nucleation controlled(stepped surface) Si films and those in Si films prepared by conventional(flat surface) solid phase crystallization. Thickness of the active region was 100nm.

This work suggests that the step-induced sold phase crystallization is useful even for super thin film Trs if we design a devices including steps with suitable shape.

Acknowledgments

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