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Dislocation Engineering for Silicon Devices

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The formation of secondary defects following ion implantation can be suppressed in several novel ways. Devices fabricated using either multiple implant steps or co-implanted carbon are shown to have higher yields than standard devices.

Damage from ion implantation in Si can lead to dislocation formation during subsequent thermal annealing.[1)] These dislocations may sharply degrade device performance, making it desireable to suppress their formation. We have demonstrated for a wide range of ion energies and ion masses that the critical parameter is the total number of silicon atoms displaced by the implant.[2)] These displaced atoms provide the mobile Si interstitials which agglomerate to form dislocations. The critical number of displaced atoms depends on the ion mass, increasing from 10^{16} /cm^2 for B to 10^{17} /cm^2 for Sb.

Knowing that a certain amount of damage is required to form dislocations suggests several ways to suppress dislocation formation for high dose implants. One method is to perform the implant in several sub-critical steps, annealing out the damage after each step. This has been demonstrated for the common dopants B, P, and As,[3)] as illustrated in Fig. 1 for 1 MeV P.

The second method for suppressing dislocation formation relies on the curious behavior of carbon implants, which do not lead to dislocation formation even for damage levels far above what is required for boron. This has been attributed to carbon atoms being able to getter some number of Si interstitials.[4)] We have demonstrated that implanting carbon over a dopant implant can suppress dislocation formation.[5)] Figure 2 shows that dislocations appear after annealing of a 1×10^{14} /cm^2 725 keV B implant, but are not present if an additional 5×10^{14} /cm^2 800 keV C implant is performed.

Both of these dislocation engineering schemes have been applied to a 4×10^{13} /cm^2 1.5 MeV P implant used to create the collector in a vertical bipolar transistor process. In these devices, dislocations may increase the leakage current and even lead to collector-emitter shorts. Figure 3 shows that the number of non-leaking transistors for either method is drastically increased compared to the standard process.

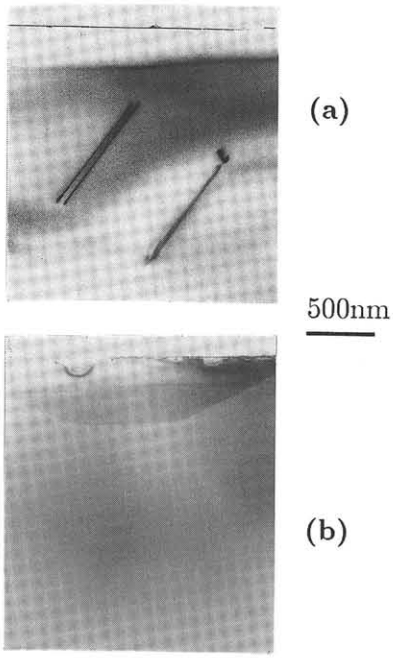

Fig. 1: Cross-section transmission electron micrographs of silicon implanted with 1×10^{14} /cm^2 1 MeV P in either (a) 1 or (b) 4 steps, with each step followed by a 900°C anneal for 15 min. No dislocations remain in the sample implanted in 4 steps.

Another implication of a critical amount of damage is that restricting the size of the implanted area should help suppress dislocation formation by, for example, increasing the out-diffusion of point defects from the damaged region. We will show that implanting into sub-micron circles drastically lowers the dislocation density compared with lines of a similar width. These examples show that an understanding of the parameters leading to dislocation formation from ion implant damage results in ways to avoid their formation and thereby increase device yield.

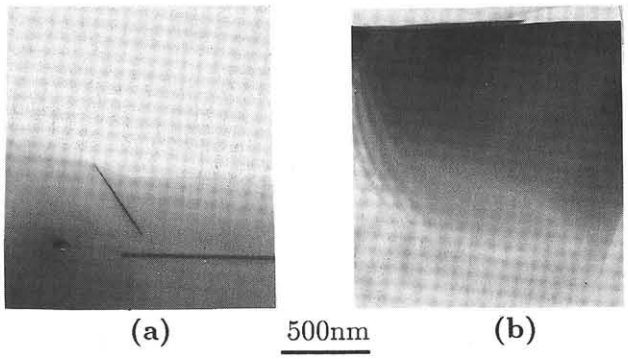

Fig. 2: Cross-section transmission electron micrographs of silicon implanted with either (a) $1 \times 10^{14}/\mathrm{cm}^2$ 725 keV B or (b) the B implant plus $5 \times 10^{14}/\mathrm{cm}^2$ 800 keV C, then annealed at 900°C for 15 min. No dislocations remain after annealing of the combined B+C implant.

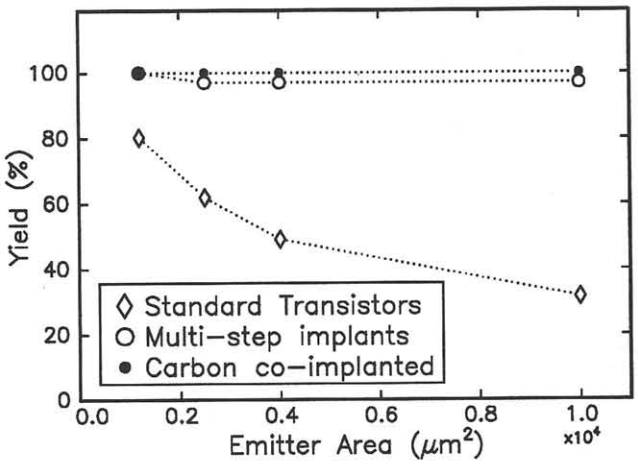

Fig. 3: Transistor yield as a function of emitter area for vertical transistors with a collector implant of $4 \times 10^{13}/\mathrm{cm}^2$ 1.5 MeV P performed in one implant (standard cell), two seperate implants (2-step implant), or with additional C implanted over the P profile (+ carbon). Either scheme to reduce dislocation formation results in significantly higher device yield.

References

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