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Evaluation of Localised Trapped Charge and Interface States in MOSFET's Through Gate Capacitances Measurement

R.Ghodsi[1], Y.T.Yeow[1], C.H.Ling[2], M.K.Alam[3]

1 Department of Electrical Engineering, the University of Queensland, AUSTRALIA
2 Department of Electrical Engineering, National University of Singapore SINGAPORE
3 School of Microelectronic Engineering, Griffith University, AUSTRALIA

This paper presents experimental and simulation study of the effect of spatially distributed trapped charge and interface states on the gate capacitances of p- and n-MOSFET's. These charges affect the capacitances through their influence on the channel potential profile. The results indicate that changes in the capacitances induced by the charges are large compared to corresponding changes in the drain current. It is also shown that the gate capacitance measurement can differentiate between trapped charges and interface states.

1. Introduction

Degradation of MOSFET's by electrical stressing is due to trapped charges or interface states in the $Si-SiO_2$ interface generated near the drain [1-3]. Both cause changes in channel potential near the drain. As gate capacitance associated with a junction is a reflection of the change in channel potential profile in response to an ac signal applied at that junction, measurement of the capacitance can shed light on the location and nature of the trapped charge. In this paper we present experimental results to show the effect of trapped charges and interface states on the gate capacitances of MOSFET's. These effects are then simulated for comparison with the experimental results.

2. Experimental and Simulation Results

The gate-to-drain and gate-to-source capacitances of p- and n-channel MOSFET's were measured with a Hewlett -Packard 4275 LCR meter as a function of the dc bias before and after electrical stressing[4]. Fig. 1 shows capacitances at the stressed junction of a p-MOSFET with $L_{eff} = 0.55\ \mu m$. C^s_{gd} and $C^s_{gd^*}$ are the gate-to-drain capacitance before and after stress, C^d_{gs} and $C^d_{gs^*}$ are the gate-to-source capacitance at the same junction, again before and after stress. Increase in the capacitance after stress is attributed to negative charge trapped in the gate oxide next to the stressed junction as shown in the insert in Fig. 1. The negative charge lowers the local V_T and leads to a lower resistance in that part of the channel. Fig. 2 (a) shows the measurement of $C^s_{gd^*}$ and the variation of the ac signal $V_{ac}(x)$ across the channel. The case of a fresh device is shown in Fig. 2(b). In each case the capacitance is given by:

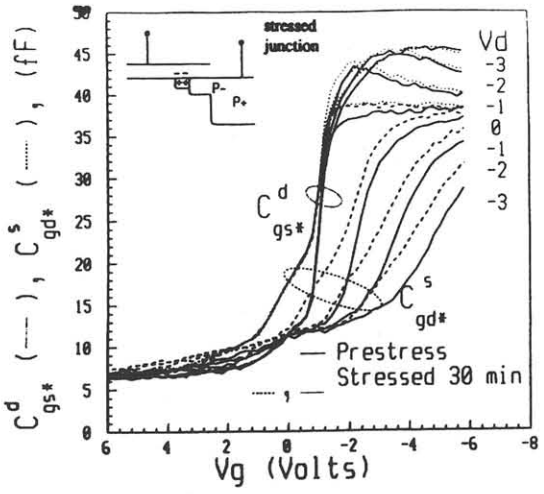

Figure1. Measured $C^d_{gs^*}$ and $C^s_{gd^*}$ versus V_g for p-MOSFET Stress conditions: $V_d = -8V, V_g = -2V$, stress time = 1800 s

$$C^s_{gd} = \frac{W \cdot C_{ox}}{V_{sig}} \cdot \int_{x=0}^{x=L} V_{ac}(x)dx$$

where C_{ox} is gate oxide capacitance per unit area, W is width of transistor, L is length of transistor, and x is distance along the channel from source to drain. The integral in this equation is the shaded area of the graphs in Fig. 2. It is seen that the $C^s_{gd^*}$ is larger than C^s_{gd}. The most significant change in Fig. 1 is the $C^s_{gd^*}$ for $V_d = 0V$. It increases just below $V_T(\approx -0.8V)$. This is due to the negative trapped charge inverting the channel below it, thus extending the drain or shortening the channel length. This is a direct observation of the channel length shortening reported previously by V-I measurement [5]. By the same reasoning we also expect $C^d_{gs^*}$ to be greater than C^d_{gs}. This increase is in general smaller due to the

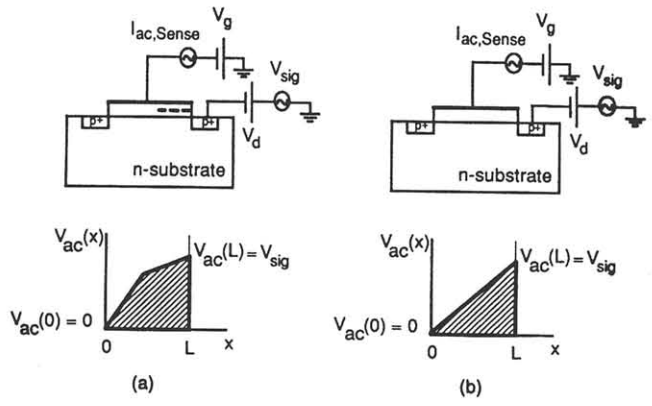

Figure 2. Measurement process for $C^s_{gd^*}$ and ac channel potential profile: (a) with negative trapped charge near measured junction, (b) with no trapped charge.

near the drain and the change of the channel resistance induced by the trapped charge near the source has a much less effect on the channel potential profile. It is also of interest to note that for $V_d = 0$ V, the $C^d_{gs^*}$ (which is also $C^s_{gd^*}$ at $V_d = 0$) shows a negative slope in the inversion regime. This is because of the fact that the trapped negative charge leads to a channel potential profile similar to the situation when $V_d < 0V$.

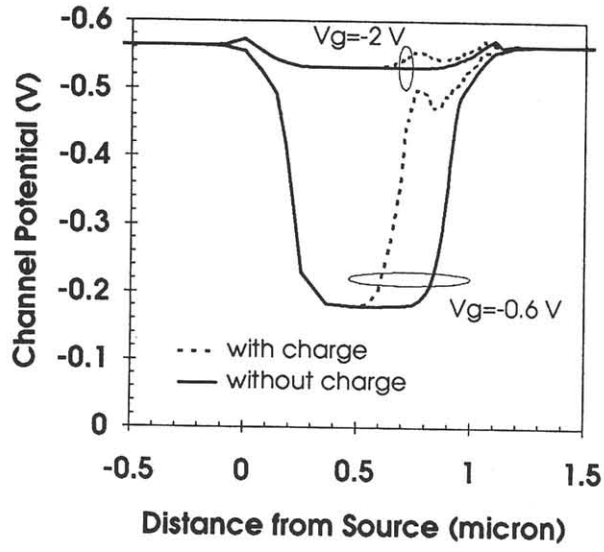

Figure 3. Simulated channel potential profile for p-MOSFET with and without trapped charge. $V_g = -0.6V$ (depletion), $V_g = -2.0V$ (inversion). $V_d = 0V$.

The actual changes in the gate capacitances are dependent on the magnitude, location and distribution of the trapped charge and on the bias condition of the transistor. The changes cannot be determined analytically. MINIMOS [6] was used to simulate the effect of trapped charges on the gate capacitances in a p-MOSFET ($L_{eff} \approx$ 0.8 μm). A Gaussian trapped charge with a peak of $-1 \times 10^{12} q\ cm^{-2}$ and a $\sigma = 0.1\ \mu m$ located at 0.15 μm from the drain edge was assumed. The effect of the trapped charge on the channel potential is shown in Fig. 3, for depletion ($V_g = -0.6V$) and for inversion ($V_g = -2.0V$). It is evident that the trapped charge has a greater effect on the channel potential in depletion than in inversion. The simulated capacitance–voltage plot is shown in Fig. 4.

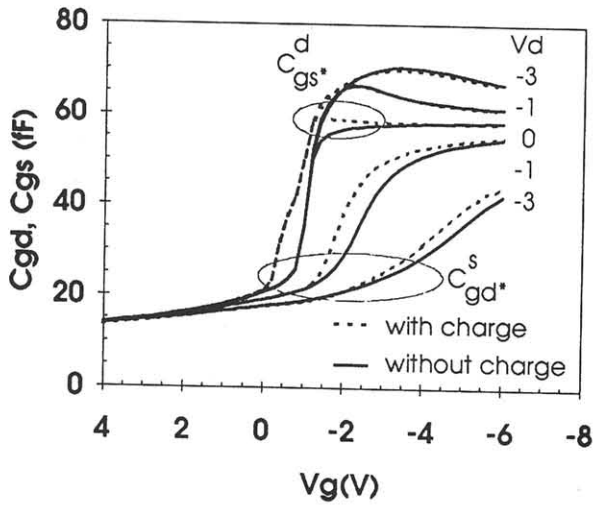

Figure 4. Simulation $C^d_{gs^*}$ and $C^s_{gd^*}$ versus V_g for p-MOSFET with trapped charge. See text for trapped charge distribution.

It shows the general features of the experimental curves, in particular the increase in $C^s_{gd^*}$ (at $V_d = 0$) below V_T. The simulated subthreshold current is shown in Fig. 5.

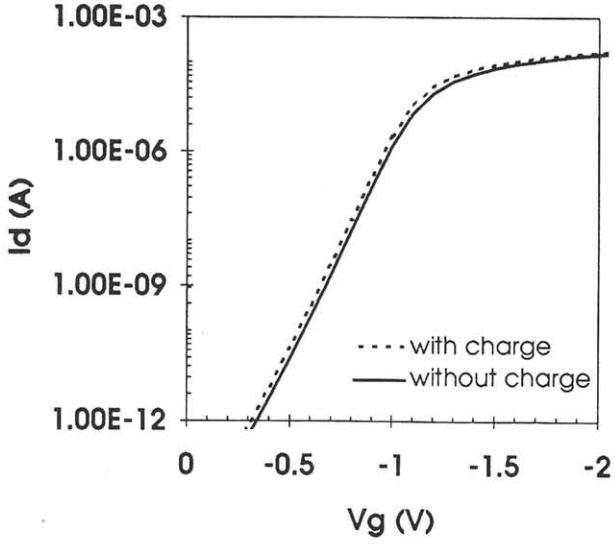

Figure 5. Simulated I_d–V_g for p-MOSFET with and without trap charge, $V_d = 100\ mV$. See text for trapped charge distribution.

As expected the trapped charge caused a shift in the I–V plot along the voltage axis. However the shift is

considerably less than the change which is observed in the capacitance–voltage plot.

Depending on the stress condition, interface states and/or trapped charges are created in the interface[3]. The charge in the interface states changes with bias whereas trapped charge is independent of bias. Fig. 6 shows experimental C^s_{gd} and $C^s_{gd^*}$ at $V_d = 0V$ for a n–MOSFET with $L_{eff} = 0.8\mu m$. For $V_g < V_T(\approx 1V)$, $C^s_{gd^*} > C^s_{gd}$ this is an indication of the presence of positive charge. For $V_g < V_T$, $C^s_{gd^*} < C^s_{gd}$ which indicates negative charge. A possible cause for the observation is that there are donor states below the midgap and acceptor states above the midgap. For V_g below V_T, the surface is accumulated, the donor states are ionised and the acceptor states are neutral, giving rise to the positive charge. Above V_T, the

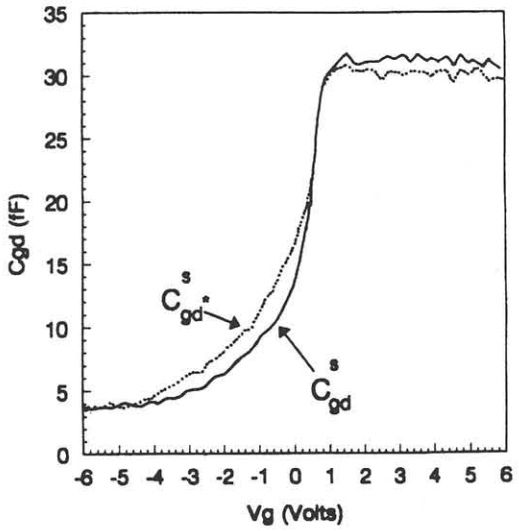

Figure 6. Measured $C^s_{gd^*}$ for n–MOSFET at $V_d = 0V$. Stress conditions: $V_d = 8V$, $V_g = 1.1V$, stress time = 10,000 s.

donor states are neutral and the acceptor states are ionised, hence the negative charge. The capacitance data therefore reflect both the spatial distribution and distribution across the band gap of the interface states. The presence of the above interface state distribution has been attributed by Pointdexter as the manifestation of the amphoteric PbO centres introduced at the Si-SiO_2 interface[7].

We simulated the interface states shown in the insert of Fig. 7. Spatially these states have a Gaussian distribution with the peak at the drain edge of the channel and $\sigma = 0.1\mu m$. As the assumed interface states distribution is not likely to be that created in the experimental device, we would not expect close matching of the simulation data in Fig. 7 with the experimental data in Fig. 6. The two graphs however show the same trend. It is seen from this simulation that the effect of interface states is low when the device is in accumulation and depletion and high for device in inversion. This is because in accumulation, the ac potential applied to the drain (or source) is not coupled to the section of the channel affected by the ionised donor states.

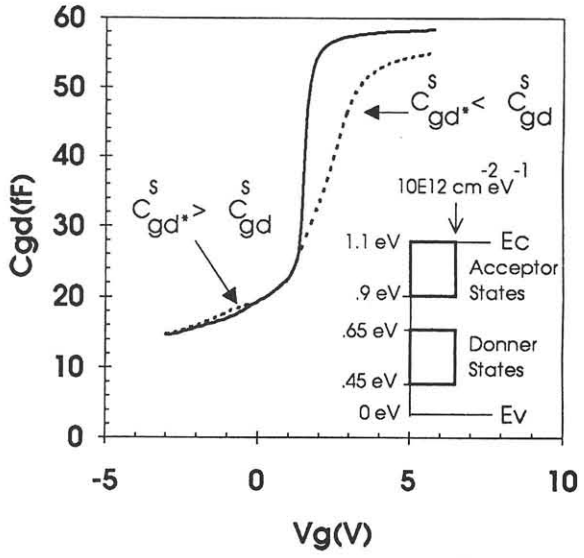

Figure 7. Simulation $C^s_{gd^*}$ for n–MOSFET with interface states at $V_d = 0V$. See text for assumed interface states density distribution.

3. Conclusions

We have studied experimentally and by simulation the effects of trapped charge and interface states on the gate capacitances of MOSFET's. It is concluded that gate capacitance measurement is a good tool for the study of these charges. It complements the I–V and charge–pumping measurement currently used to study the effect of electrical stressing of these devices. Our simulation results show that the effect of trapped charges and interface states on gate capacitances (and on the other device characteristics) are complex and that numerical simulation is essential to arrive at a model for these charges which will reflect the changes in the gate capacitances as well as the changes in the I–V data.

4. References

[1] K.K.Ng and G.W.Taylor, IEEE Trans. Electron Devices, ED-30 (1983) 871.

[2] T.Tsuchiya, T.Kobayashi and S.Nakajima, IEEE Trans. Electron Devices, ED-34 (1987) 386.

[3] P.Heremans, R.Bellens, G.Groeseneken and H.E.Maes, IEEE Trans. Electron Devices, ED-35 (1988) 2194.

[4] Y.T.Yeow, IEEE Trans. Electron Devices, ED-34 (1987) 2510.

[5] I.Kato, H.Horie, M.Taguchi and H.Ishikawa, IEDM Tech Dig., (1988) 14.

[6] W. Hänsch, S. Selberherr, IEEE Trans. Electron Devices, ED-34 (1987) 1074.

[7] E. H. Pointdexter, Semicond. Sci. Technol. 4 (1989) 961.