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A New Prediction Method for Hot Carrier Degradation of Submicron PMOSFET with Charge Pumping Technique

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We propose a new prediction method for PMOS hot carrier degradation using a charge pumping technique. In order to isolate the electron/hole (e/h) injection effect, PMOSFETs with pure, N_2O, NH_3 nitrided gate oxide films were subjected to three kinds of DC stress. These films have different immunities to e/h injection. It is found that hot carrier degradation is not due to fast-hole-induced interface states, but is mainly attributable to later electron trap degradation.

1. INTRODUCTION

High-performance PMOSFETs are the key in scaling down CMOSFETs to the deep submicron regime. However, one of the limiting factors is trap-induced degradation due to hot carrier injection. To date, several models including oxide traps and interface state generation have been reported[(1)(2)], but many discrepancies still remain.

In this paper, we demonstrate for the first time a one-to-one correlation between the oxide trap charges (ΔN_{ot}), the interface trap states (ΔN_{it}) and transconductance degradation [$\Delta g_m = g_m$(after stress)-g_m(initial)] after hot carrier injection in submicron PMOSFETs.

2. EXPERIMENTS

To investigate the electron/hole injection effect, three kinds of surface-channel PMOSFETs (N^+poly-gate, single-drain, $L_{eff}=0.8\mu m$, $W_{eff}=10\mu m$) with 10nm-thick gate SiO_2 films, RTO(#1), RTN(#2) and RTON(#3) SiO_2 films, were used. Table 1 shows the preparation sequences employed in this study. An accumulation of N atoms was found at the SiO_2/Si interface. These PMOSFETs were subjected to drain-avalanche-hot-carrier [DAHC; V_d=-8V, V_g=-2V, at $I_{g\text{-}max}$ (maximum gate current)], channel-hot-hole (CHH; $V_d=V_g$=-8V) and Fowler-Nordheim (FN; J=50mA/cm^2, V_g:positive, source/drain:open) injections. The charge pumping current (I_{cp}) [f=500kHz, ΔV_g=4V, V_r(source, drain reverse bias)=-0.1V] and maximum transconductance degradation (Δg_m, V_d=-0.1V) were monitored in this study.

3. RESULTS and DISCUSSION

Figure 1 shows I_{cp} vs gate pulse base level (V_{base}) characteristics before and after DAHC stress for the samples (#1)-(#3). For RTO(#1), I_{cp} at V_{base}=-1.8V increases at the initial stage (<1msec), and later increases at +0.2V in V_{base}. In contrast, a large increase in I_{cp} from V_{base}=-1.8V to +0.2V is found in the RTN(#2) PMOSFETs. Much smaller I_{cp} is seen in RTON(#3) for the V_{base} in the range of -4.0 to +2.0V. It is noted that I_{cp} at V_{base}=+0.2V in the RTON(#3) is smaller than that of RTO(#1) PMOSFETs. This is due to the fact that the RTON(#3) is superior[(3)(4)] to RTO(#1) in electron injection. It should be noted that there are two types of interface trap generation mechanisms. These results indicate that the I_{cp} increase at V_{base}=-1.8V is a donorlike interface trap state due to trapped holes near the drain edge. The second I_{cp} increase at V_{base}=+0.2V is attributed to an acceptorlike state resulting from trapped electrons close to the SiO_2/Si interface.

Figure 2 shows I_{cp} change after CHH injection for samples (#1)-(#3). Although the I_{cp} at

Table 1 Preparation sequences employed in this study.

No.	T_{ox}	RTO	RTON (RTN)	N (SIMS)
#1	10nm	O_2 , 1100°C 30s		5.0×10^{19} atoms /cm^3
#2	10nm	O_2 , 1100°C 30s	→ NH_3 , 1000°C , 10s	1.1×10^{22}
#3	10nm	O_2 , 1100°C 13s	→ N_2O , 1100°C , 30s	4.0×10^{21}

RTO (#1) RTN (#2) and RTON (#3)

-1.8V indeed increases for all samples, I_{cp} does not differ very much among the three PMOSFETs. Moreover, the I_{cp}-characteristics and ΔI_{cp} order in CHH stress are quite similar to those in the range of V_{base}=-6V to 0V for DAHC stress (except for #2). The gm value is scarcely changed at all CHH injections (10000sec) for all PMOSFETs. Therefore, donorlike interface states are generated by hot hole injections, but are not the major reason for PMOS (DAHC) degradation.

Figure 3 shows I_{cp} change after FN injection for samples (#1)-(#3). For RTN(#2), a large increase in I_{cp} is found at V_{base}=-6V to 4V as in DAHC injections. The ΔI_{cp} in RTON(#3) is smaller than that in RTO(#1) at V_{base}=-4V to 0V. Therefore, acceptorlike interface states are generated by hot electron injections and are the major reason for PMOS degradation.

It is clear that electron trap generation directly affects the I_{cp} change in the DAHC stress. Therefore, PMOS degradation (=ΔI_{cp}) can be separated into two factors:

$$\Delta I_{cp} = k_1 \int \Delta N_{it}\, dV_{base} + k_2 \int \Delta N_{ot}\, dV_{base}$$

where ΔN_{it} is interface state generation by hot holes and ΔN_{ot} is that due to electron traps.

Figure 4 shows the two contributions to I_{cp} characteristics for RTO(#1), RTON(#3) and RTN(#2). The initial increase in I_{cp} originated in a trapped hot hole at the interface, whereas the slow increase in I_{cp} after 1sec was caused by electron traps, which are strongly dependent on the oxide film formation. The Δg_m by DAHC stress is shown in Figure 5. From Figure 1 and Figure 5, the one-to-one correlation between ΔI_{cp} (V_{base}=+0.2V) and Δg_m is confirmed. We have observed that in RTN(#2) SiO_2 film a large number of NH and SiH bonds (electron trap sites) are generated near the SiO_2/Si interface[3,4]. In contrast, only strong SiN bonds were observed in RTON(#3) SiO_2 film. Accordingly, electron trap generation is much

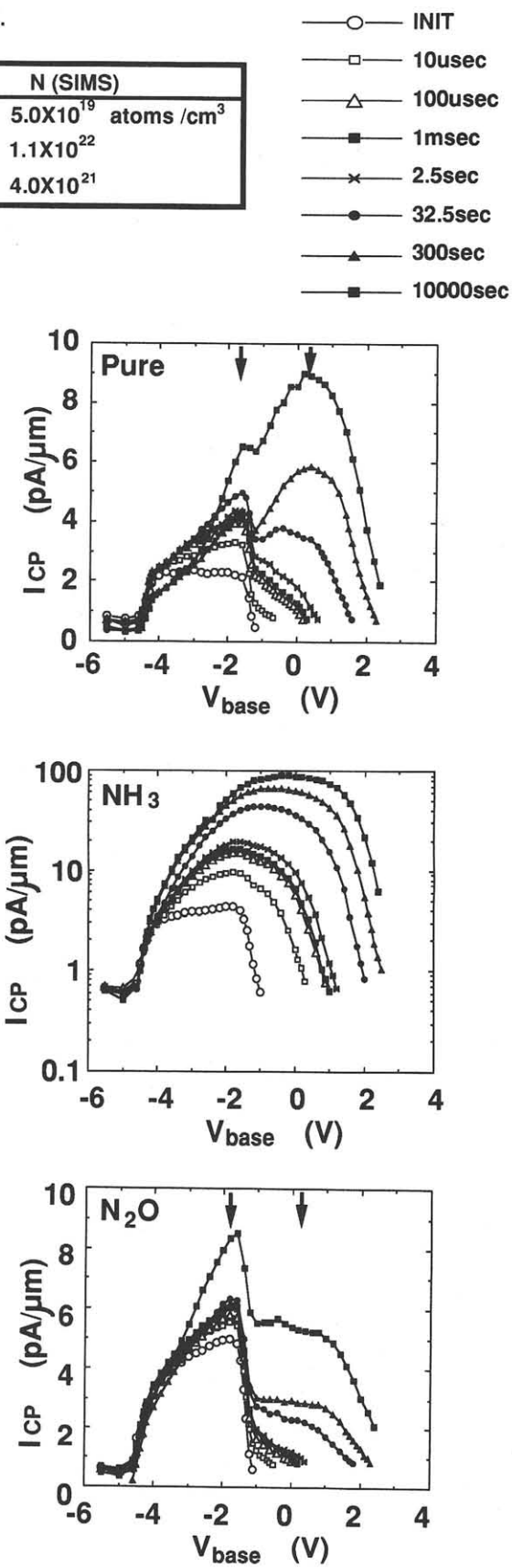

Fig.1 Charge pumping characteristics before and after DAHC stress for RTO(#1), RTN(#2) and RTON(#3) PMOSFETs.

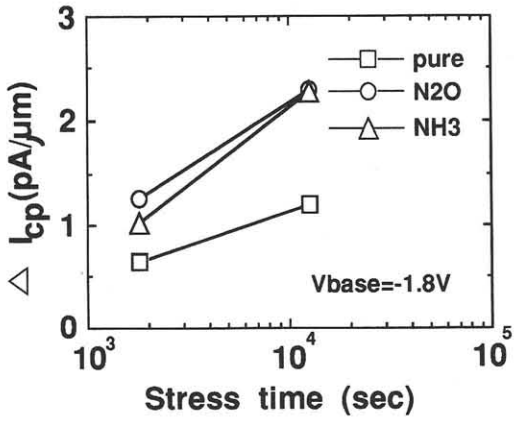

Fig.2 Increase in charge pumping current (ΔI_{cp}) after CHH stress for samples (#1)-(#3).

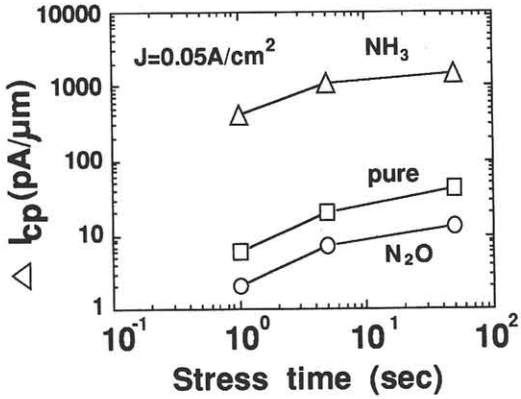

Fig.3 Increase in charge pumping current (ΔI_{cp}) after F-N stress for samples (#1)-(#3).

smaller than in RTO(#1) and RTON(#3) films.

4. CONCLUSIONS

We have studied hot carrier degradation for submicron PMOSFETs using a charge pumping technique. By this method, it can be clarified that in DAHC stress the time-dependent gm degradation is not due to a fast hole-induced interface state, but is mainly attributed to later electron trap generation. This model is consistent with p^- layer generation due to electrons (HEIP model[5]). Thus, degradation in submicron PMOSFETs can be predicted by charge trapping behavior.

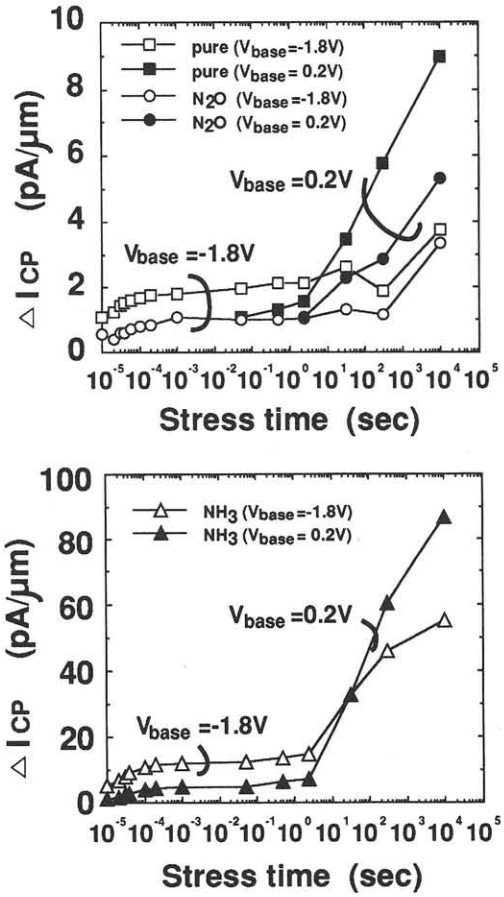

Fig.4 The I_{cp} vs DAHC stress relationships for RTO(#1), RTN(#2) and RTON(#3) PMOSFETs.

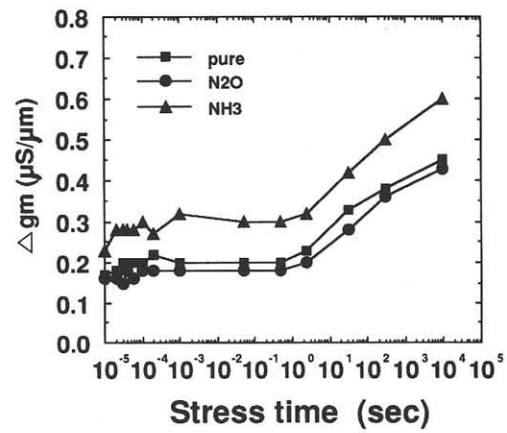

Fig.5 Maximum-transconductance degraded (gm(t)-gm(init)) as a function of stress time for RTO(#1), RTN(#2) and RTON(#3) PMOSFETs.

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