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Understanding of Enhanced Sensitivity to Hot Carrier Degradation in Drain Engineered n-FETs

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Various drain engineering techniques have been proposed for submicron CMOS devices to reduce high electric field. In this paper, we demonstrate that the enhanced device degradation due to Hot-Carrier (HC) is very sensitive to the drain doping profile near gate-to-drain overlap region. The enhanced device degradation, decrease of channel current and increase of Gate-Induced Drain Leakage (GIDL), is found to be more significant in Lightly Doped Drain (LDD) than in abrupt junction and Fully Overlap Lightly Doped (FOLD) drain devices. The enhanced device degradation in LDD devices is shown to be due to the fact that the HC damages locate outside the gate-to-drain overlap region where damage-induced barrier cannot be suppressed by the applied gate voltage. The significant increase of Band-To-Band (B-T-B) tunneling currents observed in LDD devices is shown to be caused by the fact that the HC damage is located at where the maximum field for B-T-B tunneling current occurs.

I. INTRODUCTION

Several drain engineering techniques, such as LDD [1] and FOLD [2], have been employed for submicron CMOS devices to reduce the drain electric field. The substrate current,commonly used as an indicator of the drain electric field and HC damages, can be reduced if an appropriate drain structure is chosen. However, in this paper, we demonstrate that hot carrier induced device degradation in n-FETs, decrease of drain current and increase of gate induced drain leakage (GIDL), is not only dependent on the substrate current but also very sensitive to drain doping profiles and gate-to-drain overlap structures. There is very few report and limited result [3] on the sensitivity of device characteristics to HC degradation in different drain engineered devices. For the first time, by using two dimensional device simulation along with the experimental observation, the insight of the HC damage location and its effect on the channel current degradation and GIDL in the devices with different drain structures is provided.

II. EXPERIMENTS

N-channel devices with four different drain structures are investigated, (A) As doped abrupt source/drain (S/D), (B) As doped abrupt S/D with Sb S/D extension, (C) LDD, and (D) Inverse-T FOLD (IT-FOLD). The device cross sections and process parameters for various drain structure are listed in Fig. 1. In structure A, the abrupt S/D is formed by 25 KeV, $3x10^{15}$ /cm^2 As implantation after formation of 50nm sidewall; in structure B, the S/D extension is formed by 12 and 20 KeV, $4x10^{14}$ /cm^2 Sb implantation after 10nm poly reoxidation followed by 25 KeV, $3x10^{15}$/cm^2 As implantation after 100nm sidewall; in structure C, the LDD is formed by 20 KeV, $2x10^{13}$ /cm^2 P implantation followed by abrupt As implantation. The detail process for IT-FOLD is described in [4]. All the sources and drains are subjected to 600°C and 880°C anneal post implantation. The HC stresses for all the devices are performed at the maximum substrate current condition. The reverse saturated channel current and GIDL are measured as the indicator of device degradation after stresses.

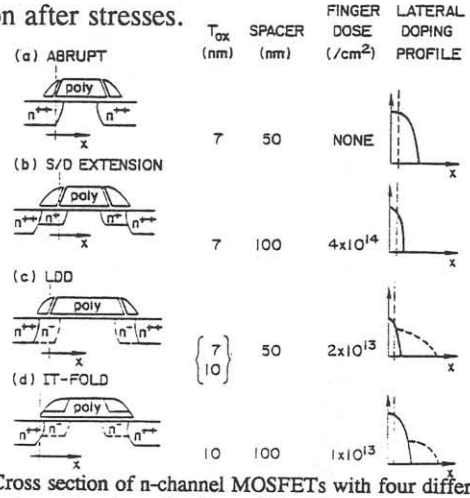

Fig. 1. Cross section of n-channel MOSFETs with four different drain engineering: (A) Abrupt S/D, (B) Abrupt S/D with extension, (C) D-FOLD, and (D) IT-FOLD.

III. RESULTS AND DISCUSSION

Due to the lightly doped drain, compared to abrupt junction devices, a 0.5V higher in stress voltage for LDD and IT-FOLD devices is needed to obtain the same substrate current as in abrupt junction and S/D extension devices. However, as shown in Fig. 2, after the HC stress with a similar substrate current, the initial drain current degradation of LDD is greater than that of devices with S/D extension and abrupt junction. The IT-FOLD devices exhibit a similar initial degradation as the abrupt S/D devices. As reported in [5], the drain current degradation can be expressed as a function of stress time by the equation $\Delta I_D / I_D = K \cdot t^n$. Here, n is the degradation rate and K is the indicator of the initial degradation. Both K and n are technology dependent. It is found that the degradation rate varies from 0.1 to 0.55 depending on the drain structure. For the abrupt junction devices, the rate is 0.55 which is in agreement with [3]. As shown in Fig. 3, the degradation rate , n, is largest in abrupt junction and IT-FOLD devices (0.55), while it is smallest in LDD devices (0.1) within a broad range of substrate current stress conditions. On the contrary, the initial degradation is the largest in LDD devices as shown in Fig. 4. Due to a larger initial degradation, the HC limited lifetime of LDD devices is shown to be significantly reduced as shown in Fig. 5. From these results, it is suggested that the HC induced degradation is very sensitive to the drain doping profile. As the doping in the gate-to-drain overlap region becomes higher, the initial HC induced degradation decreases and the degradation rate increases. These observations will be shown in the following paragraph to be due to the fact that the location of HC damage is moving out of the drain junction and toward the drain region as the doping near the drain junction decreases.

In addition to the degradation of channel current, due to the increase of negative charge in the oxide, the GIDL at a given gate-to-drain voltage also increases after HC stress. The changes of GIDL in LDD, IT-FOLD, and abrupt junction devices after subsequent HC stresses are shown in Fig. 6a, 6b, and 6c, respectively. By comparing the increase of GIDL at V_D = 2.5V and V_G = -2V, as shown in Fig. 7 the LDD device has the most significant increase of GIDL, while devices with abrupt and S/D extension has the second and the IT-FOLD device has the least. These results suggest that HC damage in LDD devices is close to the maximum field for B-T-B tunneling to modify the tunneling characteristics, while the HC damages in the other three structures are not close to the maximum field for B-T-B tunneling. As shown in insert of Fig. 6a, the simulation result indicates that in LDD the maximum field for tunneling takes place near the gate edge and in the lightly doped region where HC damage resides. Since part of HC damage is located outside the gate-to-drain overlap region, the gate voltage during the current measurement cannot suppress the

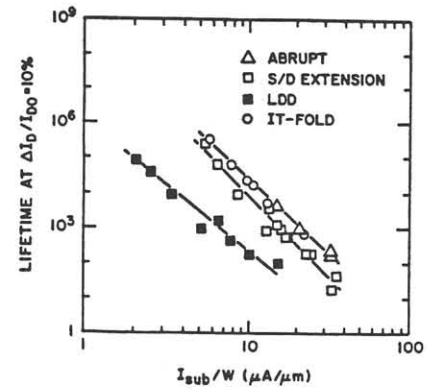

Fig. 5 Lifetime (defined as the stress time at 10% drain current degradation) of n-MOSFETs with four different drain engineering as a function of substrate current.

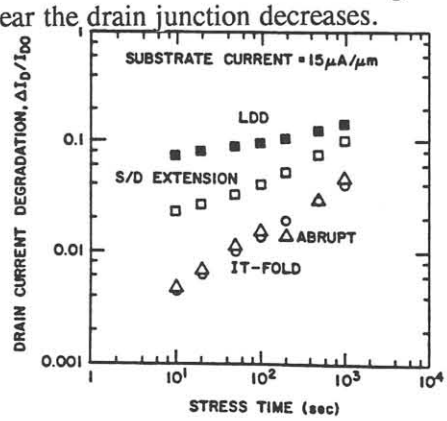

Fig. 2 Drain current degradation due to HC stress at the substrate current of 15μA/μm as a function of stress time for n-MOSFETs of four different drain structures.

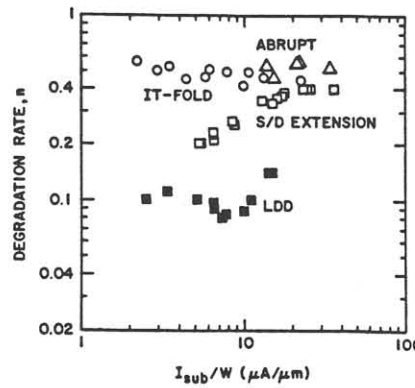

Fig. 3 Drain current degradation rate due to HC stress as a function of substrate current for n-MOSFETs of four different drain structures.

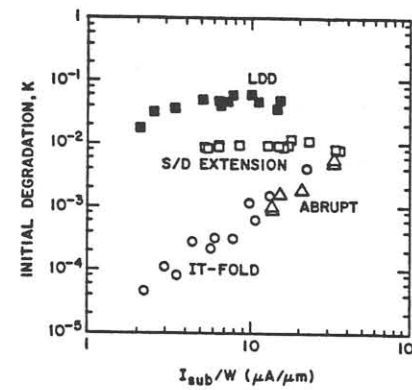

Fig. 4 Initial drain current degradation due to HC stress as a function of substrate current for n-MOSFETs of four different drain structures.

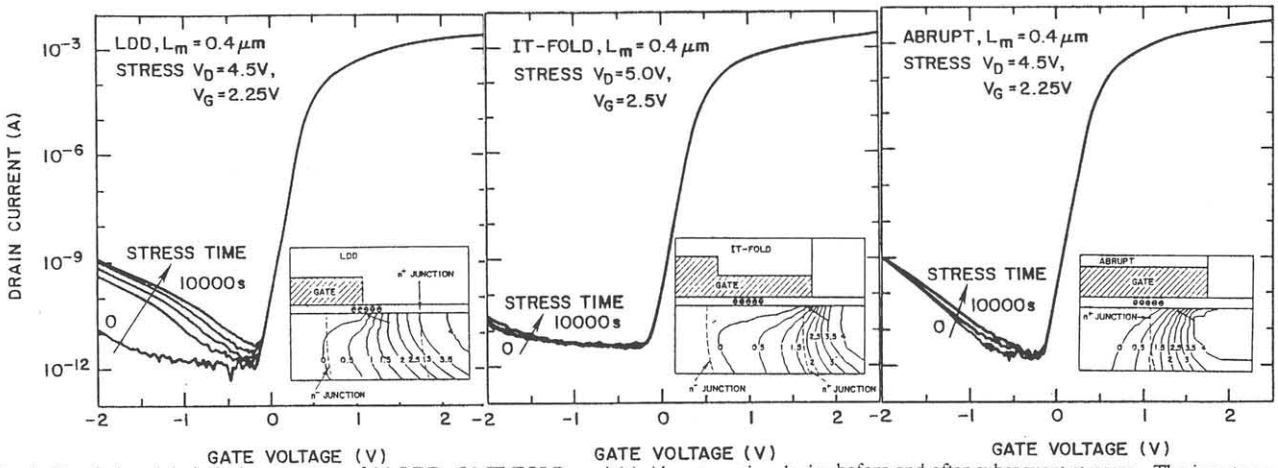

Fig. 6. Gate-induced drain leakage current of (a) LDD, (b) IT-FOLD, and (c) Abrupt unction device before and after subsequent stresses. The inserts are the potential contour to show the location of band-to-band tunneling. The arrow points at the location of B-T-B tunneling.

energy barrier induced by HC damage (as shown in Fig. 8a) and hence the channel current is significantly degraded after the initial stress. On the contrary, in IT-FOLD device, the maximum field for tunneling takes place near the junction of heavily and lightly doped regions (close to gate edge), while the HC damage locates inside the lightly doped region (underneath the gate). Therefore, the HC damage does not significantly affect the GIDL. Since the HC damage locates underneath the gate, the energy barrier induced by HC damage can be suppressed by applied gate voltage during current measurement (as shown in Fig. 8b) and hence the initial degradation is not as significant as in LDD devices. Similar explanation can also apply to the device with abrupt and S/D extension devices. In abrupt junction device, as shown in the insert of Fig. 6c, the maximum field for tunneling occurs inside the heavily doped region, while the HC damage locates near the drain junction (where maximum drain field resides during HC stress). Therefore, the channel current and GIDL degradation characteristics are similar to IT-FOLD devices.

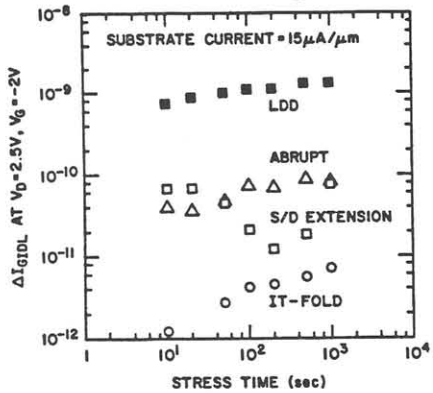

Fig. 7. The increase of GIDL of n-FETs with four different drain engineering as a function of stress time.

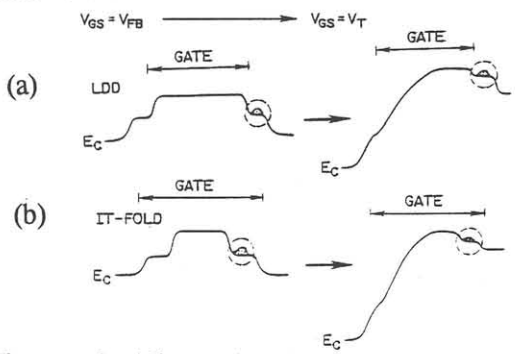

Fig. 8. The energy band diagram along the channel direction for (a) LDD and (b) IT-FOLD devices with HC damage induced barrier.

IV. CONCLUSIONS

In summary, the insights of HC damage location and its effect on the sensitivity of device degradation, decrease of channel current and increase of GIDL, are provided from experimental and simulation results. The enhanced device degradation is found to be sensitive to gate-to-drain overlap and drain doping profile. The enhanced device degradation by HC damages is observed significantly in LDD, but not in abrupt junction and IT-FOLD devices. The enhanced degradation is due to the fact that the HC damage locates outside the gate-to-drain overlap region and on top of the LDD region where damage induced barrier cannot be suppressed by the applied gate voltage. The HC damage in LDD also locates at the place where the maximum field for tunneling resides, which greatly causes the increase of GIDL. To reduce the sensitivity of device degradation to HC damage, the drain region outside the gate-to-drain overlap region must be heavily doped so that the HC damage will be inside the gate region and away from the maximum field for B-T-B tunneling. These results provide a guide line for the choice of drain engineering for high voltage and high performance submicron circuit applications.

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