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Effect of Gate Materials on Generation of Interface State by Hot-Carrier Injection

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The effect of gate materials on hot-carrier degradation, especially on the generation of the interface state, is investigated. The generation of the interface state in PMOSFET's by drain avalanche hot-carrier injection is dependent on the gate materials. The increase in interface state (ΔD_{it}) in W-gate devices is much larger than that in polycide-gate ones. It is found that this large ΔD_{it} in W-gate devices is caused by injection of electrons from the substrate. These phenomena suggest that the injection of holes from the gate into SiO_2 occurs, excited at the gate by electron injection, and is dependent on gate materials.

1. Introduction

It is known that the hot-carrier degradation of N^+ poly-Si-gate PMOSFET's is mainly caused by trapped electrons in the gate SiO_2 near the drain due to hot-electron injection. On the other hand, it is reported that positive charges and interface states are generated in MOS capacitors due to electron avalanche injection. [1] This phenomenon is explained using the surface-plasmon model. [1] The injected electrons gain energy in SiO_2. As they enter the gate electrode, this energy is lost to generate electron-hole pairs. Some of the holes have sufficient energy to tunnel back into SiO_2 and are trapped or generate the interface state. Generation and injection of holes depend on gate materials because the barrier height for holes at the gate/SiO_2 interface varies with the work function of the gate material. We reported that, when tungsten (W) is used for the gate electrode in PMOSFET, the hot-carrier degradation characteristics are quite different from those of polycide (WSi_x / N^+ poly-Si) -gate ones. [2] This difference is caused by the large increase of interface state density (ΔD_{it}) in W-gate devices. [2] In the previous report, we changed not only the gate material but also the channel doping profile in order to have the same threshold voltage (V_{th}) in W- and polycide-gate devices. Therefore, it has not been clarified whether this large ΔD_{it} in W-gate PMOSFET's is caused by the effect of gate material or the channel doping profile, which determines the hot-carrier generation and injection into SiO_2.

The objective of this work is to investigate the effect of gate materials on hot-carrier degradation, especially on the generation of the interface state. In order to separate the effect of the channel doping profile on generation of the interface state from that of gate material, W- and polycide-gate devices having the same doping profile were evaluated.

2. Experimental

W- and polycide-gate P- and N-MOSFET's having LDD structure were fabricated. The thickness of the gate oxide was 10 nm and the gate width was 10 μm. Low-stress 300 nm-thick W films [3] were deposited by magnetron sputtering. In each P- and N-MOSFET, we used two channel doping profiles of the W- and P-conditions which give $|V_{th}|$ of about 0.8 V for W- and polycide-gate devices, respectively. In PMOSFET's, devices in the W- and P-conditions result in surface- and buried-channel operation, respectively. The surface concentrations for N^- and P^- regions were the same in both devices, and were 3.9 and 3.1×10^{18} cm^{-3}, respectively.

3. Results and Discussion

The effects of stressing gate voltage (V_G) on g_m change ($\Delta g_m/g_{m0}$) in PMOSFET's are shown in Fig.1. The stress condition is in the drain avalanche hot-carrier (DAHC) injection mode. The $|\Delta g_m/g_{m0}|$ value in W-gate PMOSFET's is much smaller than that in polycide-gate ones at all values of V_G. For the purpose of comparing the characteristics of hot-carrier degradation between W- and polycide-gate PMOSFET's, the charge pumping (CP) technique [4] was adopted. Figure 2 shows CP characteristics at various V_G's before and after stressing

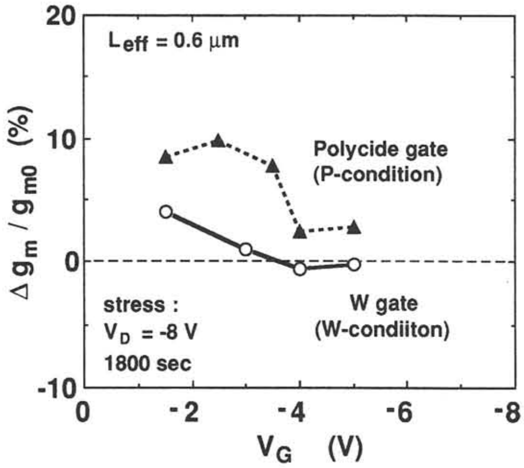

Fig.1 Dependence of $\Delta g_m / g_{m0}$ on stressing gate voltage (V_G) for **PMOSFET's**. g_m was measured at V_D = -0.1 V with exchanging source and drain after stressing.

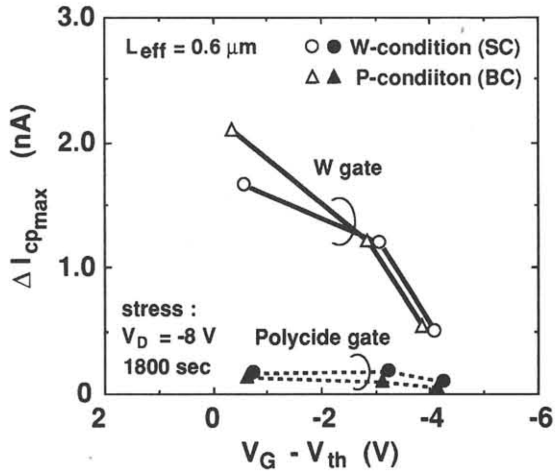

Fig.3 Dependence of ΔI_{cpmax} on V_G - V_{th} for **PMOSFET's**. The charge-pumping conditions: ΔV_A = 5 V, V_{rev}= -1 V, f = 1 MHz.

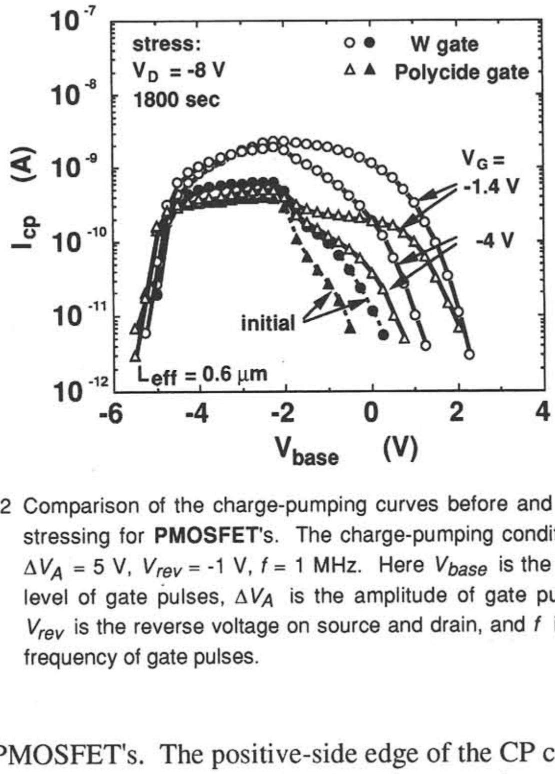

Fig.2 Comparison of the charge-pumping curves before and after stressing for **PMOSFET's**. The charge-pumping conditions: ΔV_A = 5 V, V_{rev} = -1 V, f = 1 MHz. Here V_{base} is the base level of gate pulses, ΔV_A is the amplitude of gate pulses, V_{rev} is the reverse voltage on source and drain, and f is the frequency of gate pulses.

in PMOSFET's. The positive-side edge of the CP curve shifts toward the positive direction after stressing. The shifts of W-gate devices are almost equal to those of polycide-gate ones at the same stressing condition. This indicates that the net negative charge in the gate SiO_2 of W-gate devices is almost equal to those of polycide-gate ones. However, the increase of I_{cp}, that is, ΔD_{it}, resulting from stressing is much larger in W-gate PMOSFET's than in polycide-gate ones. These results suggest that the difference in hot-carrier degradation between W- and polycide-gate devices shown in Fig.1 is mainly caused by the difference in ΔD_{it}. [2]

In order to separate the effect of the channel doping profile on generation of the interface state from that of gate material, W- and polycide-gate devices having the same doping profile were evaluated. Figure 3 shows the maximum increase of charge pumping current (ΔI_{cpmax}) as a function of V_G - V_{th} for PMOSFET's. The V_G - V_{th} is used as the abscissa because V_{th} is different in each device. Here, ΔI_{cpmax} is defined as the maximum difference between I_{cp} after and before stress. The value of ΔI_{cpmax} for W-gate devices is about 10 times larger than that for polycide-gate devices in both channel doping profiles. It is found that ΔI_{cpmax} is determined not by the channel doping profile but by the gate material. This indicates that, in PMOSFET's, ΔD_{it} is greatly affected by the gate material but is almost wholly unaffected by the difference in hot-carrier generation and injection due to the difference in the channel doping profile (in other words, a surface- or buried-channel device). On the contrary, in the case of NMOSFET's stressed under the condition of the

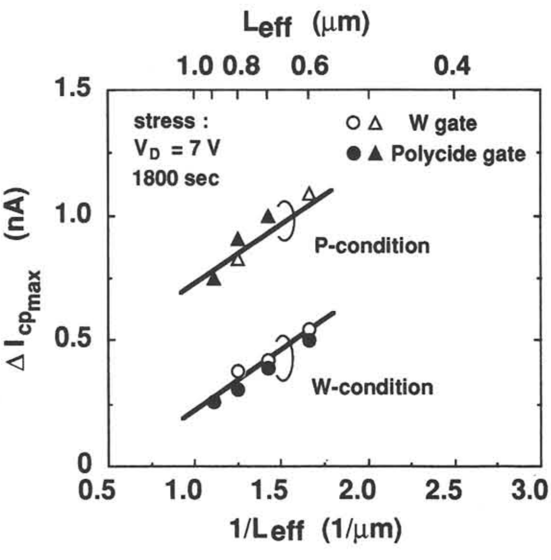

Fig.4 Dependence of ΔI_{cpmax} on L_{eff} for **NMOSFET's**. The charge -pumping conditions: ΔV_A = 5 V, V_{rev}= 1 V, f = 1 MHz.

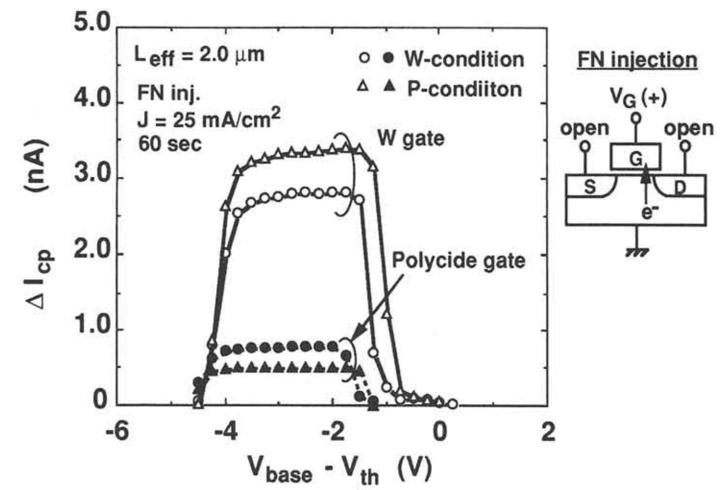

Fig.5 Comparison of ΔI_{cp} by FN injection for **PMOSFET**'s. The charge -pumping conditions: ΔV_A = 5 V, V_{rev} = -1 V, f = 1 MHz.

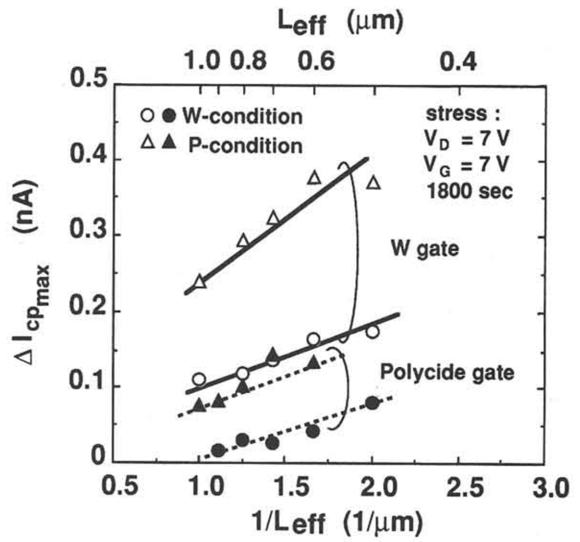

Fig.6 Dependence of $\Delta I_{cp_{max}}$ by CHE injection on L_{eff} for **NMOSFET**'s. The charge-pumping conditions: ΔV_A = 5 V, V_{rev} = 1 V, f = 1 MHz.

substrate current being maximum (DAHC injection mode), it is found that ΔIcp_{max} is independent of the gate material and is determined only by the channel doping profile as shown in Fig.4. This indicates that, in NMOSFET's, ΔD_{it} is not affected by the gate material.

The main difference in hot-carrier injection between P- and N-MOSFET's is the carrier species injected into SiO_2: electrons in PMOS and holes in NMOS for these DAHC injection modes. In order to verify the effect of carrier species injected into SiO_2, electrons were injected from the substrate to the gate electrode by FN injection in PMOSFET's. Figure 5 shows ΔI_{cp} curves by FN injection in PMOSFET's. The ΔI_{cp} of W-gate devices is much larger than that of polycide ones in both channel doping profiles. Similarly, in NMOSFET's, electrons were injected into SiO_2 by channel hot-electron (CHE) injection. Figure 6 shows the dependence of ΔIcp_{max} by CHE injection on L_{eff} in NMOSFET's. Here, ΔIcp_{max} is larger in W-gate devices than in polycide-gate ones in the same channel doping profile. These results indicate that the generation of the interface state due to electron injection is accelerated by the existence of a W-gate in both N- and P-MOSFET's. Therefore the large ΔD_{it} in W-gate PMOSFET's stressed by DAHC injection is considered to be caused by electron injection from the substrate.

Several reasons are considered as to why D_{it} in W-gate PMOSFET's is greatly increased by electron injection. One reason may be the generation of the interface state by hole injection from the gate into the gate SiO_2. The barrier height for holes at the W/SiO_2 interface is lower than that at the N^+ poly-Si/SiO_2 interface. Therefore the holes excited at the gate by the electron injection are easily injected into SiO_2 and generate many more interface states in W-gate devices than in N^+ poly-Si-gate ones. Another reason is that the property of the gate SiO_2 or SiO_2/Si interface is changed through the influence of the gate material in W-gate devices, and the interface state is easily generated by electron injection.

4. Conclusions

The effect of gate materials on hot-carrier degradation, especially on the generation of the interface state, is investigated. The generation of the interface state in NMOSFET's by DAHC injection is independent of the gate material. On the other hand, the generation of the interface state in PMOSFET's by DAHC injection is dependent on the gate material but almost independent of the channel doping profile (in other words, surface- or buried-channel device). In the case of W-gate devices, ΔD_{it} is much larger than that of polycide gate devices. It is found that this large ΔD_{it} in W-gate devices is caused by the injection of electrons from the substrate. These phenomena suggest that the injection of holes from the gate into SiO_2 occurs, excited at the gate by electron injection, and is dependent on gate materials. This degradation mode will be very important in future surface-channel PMOSFET's using gate materials other than N^+ poly-Si.

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