AC Hot-Carrier-Degradation Mechanism in LDDMOSFET's

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The hot-carrier degradation mechanism under AC stress are investigated for LDDMOSFET's. Enhanced AC degradation occurs in LDDMOSFET's as well as in single drain MOSFET's. This is explained well by the neutral-electron-trap generation model to be due to hot-hole injection, which occurs at larger VDs than a critical value. AC enhanced degradation peculiar to the LDD structure appears in gm degradation under drain voltages lower than the critical value.

1. INTRODUCTION

It has been reported that gate-pulseinduced noise from wiring inductance causes enhanced device degradation under AC stress and screen intrinsic AC effects(1)(2). After taking measures to suppress the noise, enhanced AC hot-carrier degradation was observed in single drain (SD) structure MOSFET's. The intrinsic enhanced degradation is explained well by the hot-hole-generated neutral-electron-trap model(3)(4). This model postulates that neutral electron-trap-centers are generated by hot-hole-injection during a bias condition in which drain voltages are higher than a critical value and gate voltages are low. A part of injected hot-electrons are trapped in the centers. This model is now widely accepted(5)(6). With respect to LDDstructure MOSFET's, however, opinion is almost evenly divided. Some papers say enhanced AC hot-carrier degradation is present, and others say it is not. In short, there is no universally accepted model of AC hot-carrier-degradation in LDDMOSFET's. This paper clarifies the hot-carrier-degradation intrinsic AC mechanism in LDDMOSFET's.

2. EXPERIMENTS

The devices used in this study were LDDNMOSFET's with channel widths of 20 μ m, gate lengths of 0.5 μ m, and a gate oxide thickness of 11 nm.

AC stress tests were performed by applying AC pulses to the gate electrode with a constant drain voltage. In these experiments, the influence of wiring-induced noise was prevented by connecting an external capacitor between the source and the ground. After stressing, device degradation was evaluated by threshold voltage shift ΔV th and the reduction rate in the maximum transconductance $\Delta gm/gm$ at VD=0.1 V.

3. ENHANCED AC DEGRADATION IN LDDMOSFET's

The $\Delta gm/gm$ and ΔVth dependence upon the gate voltage VG pulse rise time are shown in Fig.1(a) and (b), respectively with the stress drain voltage VD (static) as a parameter. Frequency, duty ratio, and falling time of gate pulses are fixed at 100 Hz, 50% and 50 μ sec. In order to balance the duration of both AC and DC stress, the stress time is 90 min for AC and 45 min for DC. At VD less than 5.5 V, both $\Delta gm/gm$ and ΔVth are independent of the VG gate pulse rise time. In addition, the amount of degradation due to both DC and AC stress is the same. On the other hand, at VD=6 V, both $\Delta gm/gm$ and ΔVth increase with increase in the rising time. Therefore, enhanced AC degradation appears in both ΔV th and $\Delta gm/gm$ for drain voltages higher than a critical value (6.0 V) in LDDMOSFET's, as well as SDMOSFET's.

In order to explain the reason why enhanced AC degradation generates, hot-holes and hot-electrons were alternately injected. The changes in Δ gm/gm and Δ Vth as a function of time are shown in Fig. 2. Hot holes were injected during periods I and III, hot electrons were injected during periods II, IV and VI, and trapped electrons were detrapped during period V. The changes in Δ gm/gm and



Fig. 1. (a) $\Delta gm/gm$ and (b) ΔVth as a function of stress gate-pulse rising time. Stress drain voltages are static. Frequency, duty ratio and falling time of gate pulses are fixed at 100 Hz, 50%, and 50 μ sec, respectively. Stress time is 90 min for AC and 45 min for DC.

 Δ Vth as a function of time for hot-electron injection only are shown in the insert of the figure. It is found that electron injection following hole injection causes enhanced degradation, compared with cases subjected only to electron injection. Moreover, the electron-injection-induced degradation in LDDMOSFET's is cancelled by subsequent hole injection and electron detrapping. These tendencies agree well with the case of SD structure(3). Under actual AC conditions, hotholes are injected into the oxide and generate neutral-electron-trap centers during low VG periods. Then electrons are injected during high VG periods and enhanced degradation is caused by an increase in the number of electrons trapped in the neutral-electrontraps.

For VD=6 V in Fig. 1, as the duration of hot-hole injection (i.e., the number of injected hot-holes) increases with the increase in VG pulse rise time, enhanced degradation appears in $\Delta gm/gm$ and ΔVth .

4. NEW AC DEGRADATION MECHANISM

The $\Delta g m/g m$ and $\Delta V th$ dependence upon stress frequency are shown in Fig. 3(a) and (b), respectively. Both pulse rising time and falling time are 50 nsec and duty ratio is 50%. At VD=6 V, both $\Delta gm/gm$ and $\Delta V th$ increase with increasing stress frequency. The increase in stress frequency under larger VD than the critical value shows that the number of injected holes during gate pulse rising and falling times increases. Therefore, at VD=6 V which is higher than the critical value, enhanced AC degradation appears in $\Delta V th$ and $\Delta gm/gm$, i.e, this degradation increases with increase in stress frequency. At VD=5.5 V which is less stress than the



Fig. 2. Changes in $\triangle V$ th and $\triangle gm/gm$ as a function of DC stress time.

Periods I and III: hot-hole injection (VD=6 V, VG=0.5 V); periods II, IV and VI: hot-electron injection (VD=VG=5.5 V); period V: detrapping of electrons (VD=0 V, VG=-3 V). The insert is for hot-electron-only injection.

critical value, although Δ Vth is independent of stress frequency, Δ gm/gm increases with increasing stress frequency. This is enhanced AC degradation in Δ gm/gm peculiar to the LDD structure. As shown in Fig. 4(a), even at VD values of less than the critical value, hotholes can be injected into the gate oxide above the LDD layer during low VG (the rising and/or falling edges of the gate pulse)(7). In this case, as the number of subsequentlyinjected and trapped electrons in the gate oxide above the LDD layer increases, the



Fig. 3. (a) $\Delta gm/gm$ and (b) ΔVth as a function of gate pulse frequency. Both pulse rising time and falling time are 50 nsec, and duty ratio is 50%.

resistance of the LDD layer increases, and gm is remarkably degraded. On the other hand, as Δ Vth is caused mainly by trapped electrons in the gate oxide above the channel, enhanced AC degradation does not appear in the Δ Vth. For VD values higher than the critical value, hot-holes can be injected into the gate oxide above the channel near the drain, as well as above the LDD layer, as shown in Fig. 4(b). In this case, enhanced AC degradation appears not only in Δ gm/gm but also in Δ Vth.

Here, the reason that the enhanced degradation does not appear in the $\Delta g m/g m$ for VD=5.5 V in Fig. 1(a) is the difference in the gate pulse height. Hot-carrier stress for VD=5.5 V in Fig. 1(a) is imposed at the gate pulse height which gives the maximum substrate current. This is the bias condition showing the maximum degradation rate. In this case, $\Delta gm/gm$ is caused while the gate switch is on ("gate on" period) and the effect during the rising and falling edges of the gate pulse is negligibly small.

5. CONCLUSION

AC hot-carrier effects exist in LDDMOSFET's, and are explained well by the neutral-electron-trap generation model to be due to hot-hole injection, the same as in SDMOSFET's. AC enhanced degradation peculiar to the LDD structure appears in gm degradation under drain voltages lower than a critical value, above which AC hot-carrier effects appears in the Vth shift.

ACKNOWLEDGEMENTS

The authors would like to thank Dr. Eisuke.Arai, Tetsushi Sakai and Hideo.Yoshino for their continuous encouragement through this work.



(a)For VD values less than the critical value.



(b)For VD values higher than the critical value.

Fig. 4. Schematic diagram of hole injection region for LDDMOSFET.

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