Extended Abstracts of the 1992 International Conference on Solid State Devices and Materials, Tsukuba, 1992, pp. 530-532

Electrical Properties of MOSFETs with N_2O-Nitrided LPCVD SiO_2 Gate Dielectrics

J. Ahn, G. Q. Lo, and D. L. Kwong
Microelectronics Research Center
Department of Electrical and Computer Engineering
The University of Texas at Austin, Austin, TX 78712

In this paper, the electrical properties of MOSFETs with LPCVD SiO_2 nitrided in N_2O ambient have been studied and compared to those with control thermal gate oxide. N_2O-nitridation of CVD oxides combines the advantages of interfacial oxynitride growth and defect-less nature of CVD oxides. As a result, devices with N_2O-nitrided CVD oxide show enhanced performance, improved reliability, and better TDDB property (t_{BD}).

I. INTRODUCTION

The as-deposited CVD oxide generally has inferior electrical properties for MOS gate dielectric applications due to large number of Si- and O-dangling bonds at the Si/SiO_2 interface [1]. Post-deposition annealing in O_2 and N_2 can improve CVD oxide characteristics which are close to or better than those of thermal oxide [1-3] due to a thin thermal SiO_2 formation at the Si/SiO_2 interface. Meanwhile, it has been reported that the oxidation of Si in pure N_2O ambient produces better quality oxide than thermal oxide due to [N]-incorporation at the Si/SiO_2 interface [4-5]. It can be expected that annealing of CVD SiO_2 in N_2O not only densifies CVD SiO_2 but also grows interfacial $Si_xO_yN_z$ layer.

This paper reports performance and reliability of MOSFETs with thin (~87 Å) LPCVD gate oxides nitrided in N_2O in comparison with those with control- and N_2O-nitrided thermal gate oxide. The devices with N_2O-nitrided CVD oxide shows the best performance and TDDB characteristics, while their reliability is slightly inferior to those with N_2O-nitrided thermal oxide but still better than those with control thermal oxide.

II. EXPERIMENTAL

N^+ poly-Si gate n-MOSFETs were fabricated using CMOS twin-well technology and LOCOS isolation. N_2O-nitrided CVD oxide (~87 Å) was prepared by LPCVD SiO_2 film at 450°C using SiH_4 and O_2 in a hot-wall type multi-wafer reactor followed by furnace nitridation in pure N_2O at 950°C for 10 min. Preparation of N_2O-nitrided thermal oxide (~85 Å) was described in 6). For comparison, control oxide (~85 Å) was grown in furnace with dry O_2 at 950°C followed by annealing in N_2 at the same temperature. The thickness was measured by C-V technique on adjacent MOS capacitors and by ellipsometry. Thickness uniformities across the 4"-wafers were within ±2% deviation for all oxides.

III. RESULTS AND DISCUSSION

Fig. 1 shows an Auger Electron Spectroscopy (AES) depth profile of nitrogen in CVD oxide annealed in N_2O at 950°C for 10 min. This profile shows a nitrogen peak at the Si/SiO_2 interface with a small amount of nitrogen in the bulk. This overall profile is similar to that of oxynitride film grown by thermal oxidation of Si in N_2O ambient, although the nitrogen concentration in N_2O-annealed CVD oxide is lower than that in oxynitride [4]. The thickness increase by annealing in N_2O at 950°C for 10 min was ~25 Å by ellipsometric measurement and the thickness uniformity of the as-deposited CVD oxide was significantly improved by the annealing in N_2O (within ±1.5%). A fixed refractive index (1.46) was used for ellipsometry because the [N] in the bulk oxide is small.

Fig. 2 shows time-to-breakdown (t_{BD}) distributions of MOS capacitors with different gate dielectrics characterized by applying constant field stress (11.5 MV/cm). Capacitors with N_2O-nitrided thermal and CVD oxides show much tighter distributions and higher t_{BD} values compared to those with control thermal oxide, implying much reduced weak oxide spots or defects through nitrogen incorporation at the interface [5]. Strained Si-O bonds, which are susceptible to the bond-

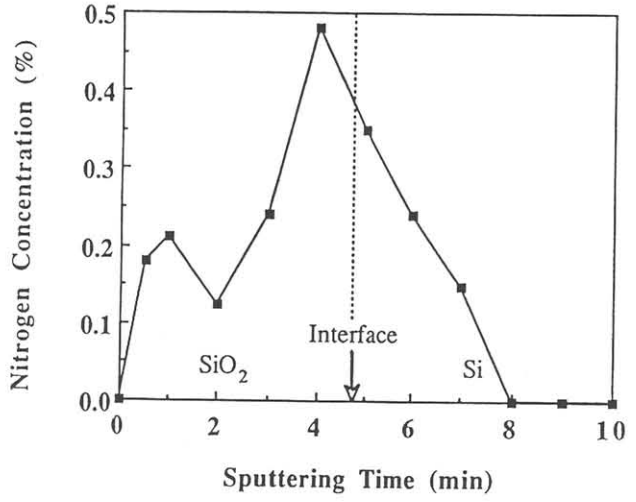

Fig. 1 AES depth profile of nitrogen for CVD oxide annealed in N_2O at 950°C for 10 min.

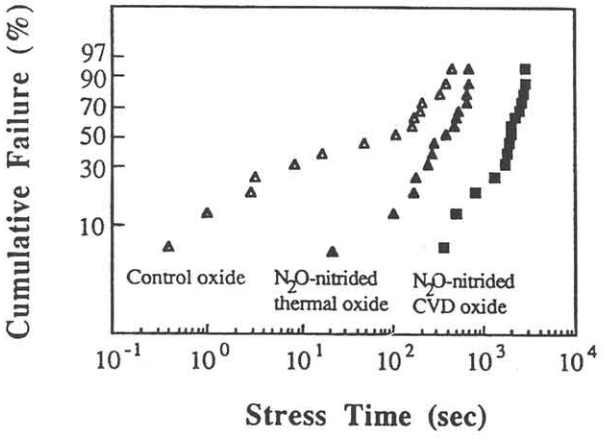

Fig. 2 Time-to-breakdown (t_{BD}) distributions of MOS capacitors (area= $5x10^{-5}$ cm^2) with different gate dielectrics characterized by applying constant field stress (11.5 MV/cm)

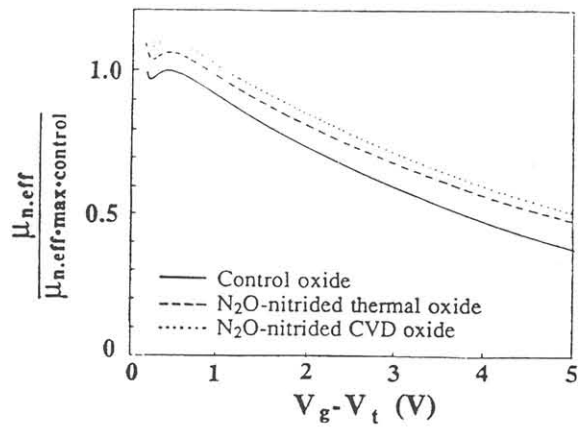

Fig. 3 Normalized effective electron mobility ($\mu_{n,eff}/\mu_{n,eff.max.control}$) as a function of ($V_g$-$V_t$) obtained from MOSFETs (W_{eff}/L_{eff}=15 μm /15 μm) with different gate dielectrics

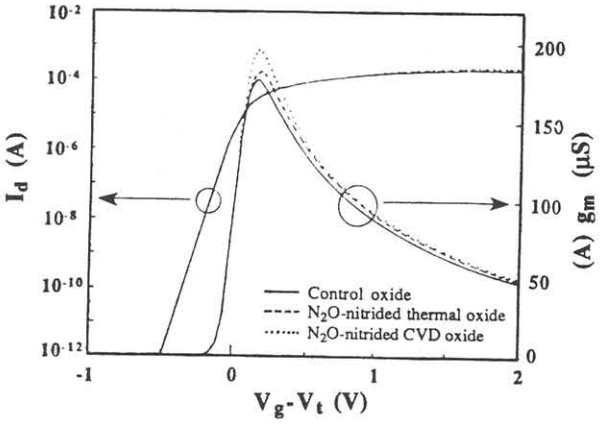

Fig. 4 I_g *vs.* V_g and g_m *vs.* V_g characteristics of submicron MOSFETs (W_{eff}/L_{eff}=15 μm/0.8 μm) with different gate dielectrics.

breaking by hot-carriers, are reduced by interfacial $Si_xO_yN_z$-formation during N_2O-nitridation. Because CVD oxide is deposited on rather than grown from the substrate without lattice match requirement [7], N_2O-nitrided CVD oxide has even less strained bonds and smaller number of defects which result in even higher t_{BD} value than in N_2O-nitrided thermal oxide.

Effective electron mobilities, defined as $\mu_{n,eff}= I_d/[V_d \cdot W/L \cdot C_{ox}(V_g-V_t)]$, in MOSFETs ($W_{eff}/L_{eff}$=15 μm /15 μm) with different gate dielectrics are normalized to the peak $\mu_{n,eff}$ of control oxide device and plotted in Fig. 3 as a function of gate drive (V_g-V_t). Both D_{it} and subthreshold slopes (S) are similar in all devices (D_{it}~ $5x10^{10}$ $cm^{-2}eV^{-1}$ and S~70 mV/dec), as shown in Fig. 4. Fixed charge densities (N_f) are $5x10^{10}$ for control and N_2O-nitrided thermal oxide devices and $7x10^{10}$ cm^{-2} for N_2O-nitrided CVD oxide device. The slightly higher N_f for CVD oxide may be a result of insufficient densification. The improvement factors of $\mu_{n,eff}$ over control oxide are ~10% for N_2O-nitrided CVD oxide and ~7% for N_2O-nitrided thermal oxide. The dependence of $\mu_{n,eff}$ on V_g-V_t is similar for all devices. It has been reported that $\mu_{n,eff}$ and g_m can be improved for all V_g by applying mechanical tensile stress to the thermal oxide which has residual compressive stress [8]. An interfacial $Si_xO_yN_z$ formation with low nitrogen concentration ($[N]_{int}$~0.5-1.5%) during N_2O-nitridation, which is believed to result in less strained interface structure than control thermal oxide interface, without any noticeable increase of N_f or D_{it}. Excessive nitrogen at SiO_2/Si interface, however, has been reported to degrade device performance (reduced $\mu_{n,eff}$ and g_m at low V_g) in NH_3-nitrided thermal oxide devices [8-10]. Recent study showed that very light NH_3-nitridation ($[N]_{int}$ ~0.5%) can solve this problem [11]. We believe that the improved $\mu_{n,eff}$ in N_2O-nitrided CVD oxide is a combined effect of

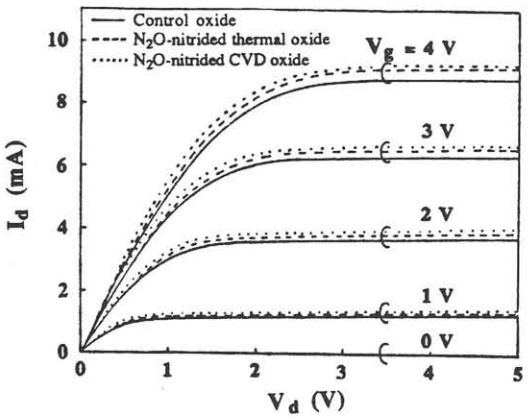

Fig. 5 Current drivability (I_d *vs.* V_d) of submicron MOSFETs with different gate dielectrics.

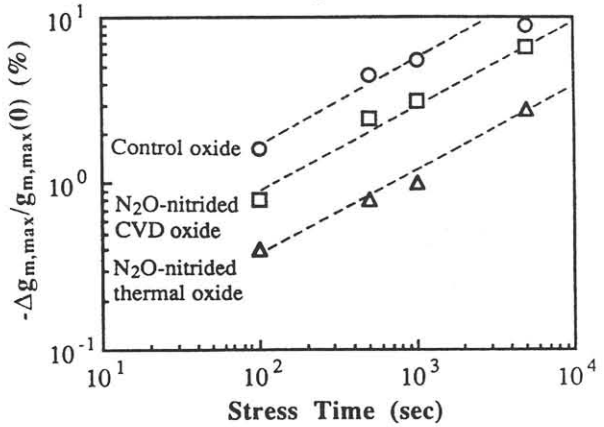

Fig. 6 Stress-time dependence of g_m degradation of submicron MOSFETs induced by channel hot carrier stress with $I_{sub,max}$ (V_g= 2.5 V, V_d= 7.5 V)

interfacial oxynitride layer growth ($[N]_{int}$ ~0.5%) and strainless nature of CVD SiO_2/Si interface [12]. As a result, current drivability is also improved in both high and low V_g ranges, as shown in Fig. 5.

Fig. 6 shows peak-g_m degradation *vs.* stress time in MOSFETs (W_{eff}/L_{eff}=15μm/0.8 μm) during channel hot carrier stress (CHCS) with $I_{sub,max}$. MOSFETs with N_2O-nitrided thermal and CVD oxides show suppressed Δg_m than MOSFETs with control thermal oxide. The ΔD_{it} during CHCS may be due to a direct bond breaking process at the interface. Substitution of strained Si-O bonds with stronger Si-N bonds during N_2O-nitridation [6] is believed to improve interface hardness, resulting in less Δg_m. The suppression is less significant in N_2O-nitrided CVD oxide than in N_2O-nitrided thermal oxide due to smaller amount of Si-N bonds at the interface ($[N]_{int}$~0.5% for N_2O-nitrided CVD oxide *vs.* $[N]_{int}$~1.5% for N_2O-nitrided thermal oxide) [11].

Fowler-Nordheim (F-N) current stress was also performed on MOSFETs, and result shows the same trend in Δg_m and threshold voltage shift (ΔV_t) as in CHCS. In Fig. 7 contributions of ΔD_{it} (ΔV_{it}) and charge trapping (ΔV_{ot}) to ΔV_t were separated by using

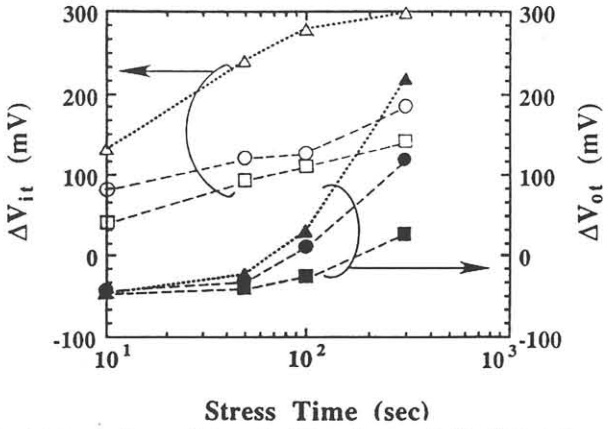

Fig. 7 Fraction of threshold voltage shift (ΔV_t) due to ΔD_{it} (ΔV_{it}) and charge trapping (ΔV_{ot}) under F-N constant current injection on submicron MOSFETs with control (triangle), N_2O-nitrided CVD (circle), and N_2O-nitrided thermal oxide (square).

subthreshold slope change (ΔS), *i.e.*, ΔV_{it}= $\Delta S \cdot \Phi_B/[kT/q \cdot \ln 10]$ and ΔV_{ot}= ΔV_t-ΔV_{it}, where Φ_B= $2\Phi_F = 2kT/q \cdot \ln (N_a/n_i)$ [13]. As can be seen, both ΔD_{it} and electron trapping are suppressed in N_2O-nitrided oxides compared to control thermal oxide.

IV. CONCLUSION

N_2O-nitridation of CVD oxide combines the advantages of defect-less nature of CVD oxide, and the strainless interfacial oxynitride growth and densification effects of N_2O-nitridation. As a result, MOS devices with this gate dielectric exhibit improved performance, enhanced reliability, and improved TDDB characteristics compared to those with control thermal gate oxide.

This work was supported by SRC/SEMATECH and Texas Advanced Technology Program

REFERENCES

1) S. Ang and S. Wilson, *J. Electrochem. Soc.*, 134, 1987, 1254
2) J. Lee et al., *IEEE Electron Device Lett.*, 1986, 506
3) J. Lee et al., *IEEE Electron Device Lett.*, 1988, 324
4) H. Hwang et al., in *IEDM Tech. Dig.*, 1990, 421
5) W. Ting et al., *IEEE Electron Device Lett.*, 1991, 416
6) J. Ahn et al., *IEEE Electron Device Lett.*, 1992, 117
7) J. Ahn et al., *IEEE DRC*, 1991, IVB-1
8) H. Momose et al., in *IEDM Tech. Dig.*, 1990, 65
9) M. Schmidt et al., *IEEE Electron Dev.*, 1988, 1627
10) T. Hori and H. Iwasaki, in *IEDM Tech. Dig.*, 1989, 459
11) H. Momose et al., in *IEDM Tech. Dig.*, 1991, 359
12) J. Ahn et al., *IEEE Electron Device Lett.*, 1992, 186
13) R. Sundaresan et al., *IEEE Trans. Nucl. Sci.*, 1986, 1223