Electrical Properties of MOSFETs with N$_2$O-Nitrided LPCVD SiO$_2$ Gate Dielectrics

J. Ahn, G. Q. Lo, and D. L. Kwong
Microelectronics Research Center
Department of Electrical and Computer Engineering
The University of Texas at Austin, Austin, TX 78712

In this paper, the electrical properties of MOSFETs with LPCVD SiO$_2$ nitrided in N$_2$O ambient have been studied and compared to those with control thermal gate oxide. N$_2$O-nitridation of CVD oxides combines the advantages of interfacial oxynitride growth and defect-less nature of CVD oxides. As a result, devices with N$_2$O-nitrided CVD oxide show enhanced performance, improved reliability, and better TDDB property ($t_{BD}$).

I. INTRODUCTION
The as-deposited CVD oxide generally has inferior electrical properties for MOS gate dielectric applications due to large number of Si- and O-dangling bonds at the Si/SiO$_2$ interface $^{1)}$. Post-deposition annealing in O$_2$ and N$_2$ can improve CVD oxide characteristics which are close to or better than those of thermal oxide $^{3,4)}$ due to a thin thermal SiO$_2$ formation at the Si/SiO$_2$ interface. Meanwhile, it has been reported that the oxidation of Si in pure N$_2$O ambient produces better quality oxide than thermal oxide due to [N]-incorporation at the Si/SiO$_2$ interface $^{1)}$. It can be expected that annealing of CVD SiO$_2$ in N$_2$O not only densifies CVD SiO$_2$ but also grows interfacial Si$_3$N$_4$ layer.

This paper reports performance and reliability of MOSFETs with thin (~87 Å) LPCVD gate oxides nitrided in N$_2$O in comparison with those with control- and N$_2$O-nitrided thermal gate oxide. The devices with N$_2$O-nitrided CVD oxide shows the best performance and TDDB characteristics, while their reliability is slightly inferior to those with N$_2$O-nitrided thermal oxide but still better than those with control thermal oxide.

II. EXPERIMENTAL
N$^+$ poly-Si gate n-MOSFETs were fabricated using CMOS twin-well technology and LOCOS isolation. N$_2$O-nitrided CVD oxide (~87 Å) was prepared by LPCVD SiO$_2$ film at 450$^\circ$C using SiH$_4$ and O$_2$ in a hot-wall type multi-wafer reactor followed by furnace nitridation in pure N$_2$O at 950$^\circ$C for 10 min. Preparation of N$_2$O-nitrided thermal oxide (~85 Å) was described in 6). For comparison, control oxide (~85 Å) was grown in furnace with dry O$_2$ at 950$^\circ$C followed by annealing in N$_2$ at the same temperature. The thickness was measured by C-V technique on adjacent MOS capacitors and by ellipsometry. Thickness uniformities across the 4”-wafers were within ±2% deviation for all oxides.

III. RESULTS AND DISCUSSION
Fig. 1 shows an Auger Electron Spectroscopy (AES) depth profile of nitrogen in CVD oxide annealed in N$_2$O at 950$^\circ$C for 10 min. This profile shows a nitrogen peak at the Si/SiO$_2$ interface with a small amount of nitrogen in the bulk. This overall profile is similar to that of oxynitride film grown by thermal oxidation of Si in N$_2$O ambient, although the nitrogen concentration in N$_2$O-annealed CVD oxide is lower than that in oxynitride $^{4)}$. The thickness increase by annealing in N$_2$O at 950$^\circ$C for 10 min was ~25 Å by ellipsometric measurement and the thickness uniformity of the as-deposited CVD oxide was significantly improved by the annealing in N$_2$O (within ±1.5%). A fixed refractive index (1.46) was used for ellipsometry because the [N] in the bulk oxide is small.

Fig. 2 shows time-to-breakdown ($t_{BD}$) distributions of MOS capacitors with different gate dielectrics characterized by applying constant field stress (11.5 MV/cm). Capacitors with N$_2$O-nitrided thermal and CVD oxides show much tighter distributions and higher $t_{BD}$ values compared to those with control thermal oxide, implying much reduced weak oxide spots or defects through nitrogen incorporation at the interface $^{5)}$. Strained Si-O bonds, which are susceptible to the bond-
Nitrogen Concentration

![Fig. 1](image)

**Fig. 1** AES depth profile of nitrogen for CVD oxide annealed in N2O at 950°C for 10 min.

Cumulative Failure (%)

![Fig. 2](image)

**Fig. 2** Time-to-breakdown (tBD) distributions of MOS capacitors (area= 5x10^-3 cm^2) with different gate dielectrics characterized by applying constant field stress (11.5 MV/cm)

break by hot-carriers, are reduced by interfacial SiO_xNy formation during N2O nitridation. Because CVD oxide is deposited on rather than grown from the substrate without lattice match requirement), N2O-nitrided CVD oxide has even less strained bonds and smaller number of defects which result in even higher tBD value than in N2O-nitrided thermal oxide.

Effective electron mobilities, defined as \( \mu_{n,\text{eff}} = \frac{I_d}{V_{gs} W/\text{Cox}(V_{gs}-V_T)} \), in MOSFETs (W/\text{L} = 15 \mu m / 15 \mu m) with different gate dielectrics are normalized to the peak \( \mu_{n,\text{eff}} \) of control oxide device and plotted in Fig. 3 as a function of gate drive \( (V_{gs}-V_T) \). Both \( D_{th} \) and subthreshold slopes \( (S) \) are similar in all devices \( (D_{th} = 5x10^{10} \text{ cm}^{-2}\text{eV}^{-1} \text{ and } S~70 \text{ mV/dec}) \), as shown in Fig. 4. Fixed charge densities \( (N_f) \) are 5x10^{10} for control and N2O-nitrided thermal oxide devices and 7x10^{10} \text{ cm}^{-2} for N2O-nitrided CVD oxide device. The slightly higher \( N_f \) for CVD oxide may be a result of insufficient densification. The improvement factors of \( \mu_{n,\text{eff}} \) over control oxide are ~10% for N2O-nitrided CVD oxide and ~7% for N2O-nitrided thermal oxide. The dependence of \( \mu_{n,\text{eff}} \) on \( V_{gs}-V_T \) is similar for all devices. It has been reported that \( \mu_{n,\text{eff}} \) and \( g_m \) can be improved for all \( V_g \) by applying mechanical tensile stress to the thermal oxide which has residual compressive stress.

An interfacial SiO_xNy formation with low nitrogen concentration \( ([N]_{int}=0.5-1.5\%) \) during N2O nitridation, which is believed to result in less strained interface structure than control thermal oxide interface, without any noticeable increase of \( N_f \) or \( D_{th} \). Excessive nitrogen at SiO_x/Si interface, however, has been reported to degrade device performance (reduced \( \mu_{n,\text{eff}} \) and \( g_m \) at low \( V_g \)) in NH3-nitrided thermal oxide devices. Recent study showed that very light NH3-nitridation \( ([N]_{int}=0.5\%) \) can solve this problem. We believe that the improved \( \mu_{n,\text{eff}} \) in N2O-nitrided CVD oxide is a combined effect of

![Fig. 3](image)

**Fig. 3** Normalized effective electron mobility \( (\mu_{n,\text{eff}}/\mu_{n,\text{eff, max, control}}) \) as a function of \( (V_{gs}-V_T) \) obtained from MOSFETs \( (W/\text{L} = 15 \mu m / 15 \mu m) \) with different gate dielectrics.

![Fig. 4](image)

**Fig. 4** \( I_g \) vs. \( V_g \) and \( g_m \) vs. \( V_g \) characteristics of submicron MOSFETs \( (W/\text{L} = 15 \mu m / 0.8 \mu m) \) with different gate dielectrics.
interfacial oxynitride layer growth ([N]_int ~0.5%) and strainless nature of CVD SiO_x/Si interface. As a result, current drivability is also improved in both high and low V_g ranges, as shown in Fig. 5.

Fig. 6 shows peak-gm degradation vs. stress time in MOSFETs (W_eff/L_eff=15μm/0.8 μm) during channel hot carrier stress (CHCS) with I_{sub,max}. MOSFETs with N_2O-nitrided thermal and CVD oxides show suppressed Δg_m than MOSFETs with control thermal oxide. The ΔD_t during CHCS may be due to a direct bond breaking process at the interface. Substitution of strained Si-O bonds with stronger Si-N bonds during N_2O-nitridation is believed to improve interface hardness, resulting in less Δg_m. The suppression is less significant in N_2O-nitrided CVD oxide than in N_2O-nitrided thermal oxide due to smaller amount of Si-N bonds at the interface ([N]_int~0.5% for N_2O-nitrided CVD oxide vs. [N]_int~1.5% for N_2O-nitrided thermal oxide).

Fowler-Nordheim (F-N) current stress was also performed on MOSFETs, and result shows the same trend in Δg_m and threshold voltage shift (∆V_t) as in CHCS. In Fig. 7 contributions of ΔD_t (∆V_t) and charge trapping (∆V_on) to ∆V_t were separated by using subthreshold slope change (∆S), i.e., ∆V_t=ΔS*Φ_F/[kT/q*ln10] and ∆V_on=∆V_t-ΔV_t, where Φ_F=2φ_F=2kT/q*ln(N/V_n). As can be seen, both ΔD_t and electron trapping are suppressed in N_2O-nitrided oxides compared to control thermal oxide.

IV. CONCLUSION

N_2O-nitridation of CVD oxide combines the advantages of defect-less nature of CVD oxide, and the strainless interfacial oxynitride growth and densification effects of N_2O-nitridation. As a result, MOS devices with this gate dielectric exhibit improved performance, enhanced reliability, and improved TDDB characteristics compared to those with control thermal gate oxide.

This work was supported by SRC/SEMATECH and Texas Advanced Technology Program.

REFERENCES

2) J. Lee et al., IEEE Electron Device Lett., 1986, 506
3) J. Lee et al., IEEE Electron Device Lett., 1988, 324
4) H. Hwang et al., in IEDM Tech. Dig., 1990, 421
7) J. Ahn et al., IEEE DRC, 1991, IVB-1
8) H. Momose et al., in IEDM Tech. Dig., 1990, 65
9) M. Schmidt et al., IEEE Electron Dev., 1988, 1627