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Nitride Masked Polishing (NMP) Technique for Surface Planarization of Interlayer-Dielectric Films

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A reflowed borophosphosilicate glass (BPSG) film having surface ridges is polished mechanically with a colloidal silica slurry, and ridge width effect on the planarization rate is investigated. The planarization rate decreases drastically with increasing the ridge width, thereby it is impossible to effectively remove wide BPSG ridges corresponding to the memory cell array areas in a DRAM device. Then, a Nitride Masked Polishing (NMP) technique is proposed in which BPSG surface except for ridge areas are covered with a Si_3N_4 film and the ridges are selectively polished away. A BPSG film on a DRAM device is planarized sufficiently by the NMP to insure a tight focus margin for photolithography below deep submicron processes.

1. INTRODUCTION

When device patterns in ULSIs are downsized to a deep submicron, surface planarization becomes very important to insure a tight focus margin for photolithography. BPSG-reflow[1], resist etch-back[2] and spin-on-glass (SOG) coating[3] processes are useful for smoothing local surface topography, but insufficient for attaining global surface planarization. Recently, polishing processes have been recognized as one of candidates for the global surface planarization[4,5].

In this paper, a reflowed BPSG interlayer-dielectric film is polished mechanically with a colloidal silica slurry, and the pattern width effect on the planarization rate of the surface ridges is investigated. Then, a Nitride Masked Polishing (NMP) technique, in which a Si_3N_4 film is used as a polishing protection layer, is proposed to planarize a BPSG film on DRAM devices.

2. EXPERIMENTAL

Figure 1 illustrates a test structure used for investigating ridge width effect on a planarization rate by a mechanical polishing. A 0.8μm-thick CVD-BPSG was deposited on poly-Si patterns with a variety of line widths (W=1μm~25μm) and fixed line length and height (L=1000μm and h=0.5μm). After heating at 850°C for 30 minutes, the BPSG film was polished mechanically with a colloidal silica slurry for one minute. Changes in the ridge height (h) and the thickness of the BPSG film surrounding the ridges (d_{BP}) were examined by surface profiler and ellipsometer, respectively.

Figure 2 illustrates test structures used for

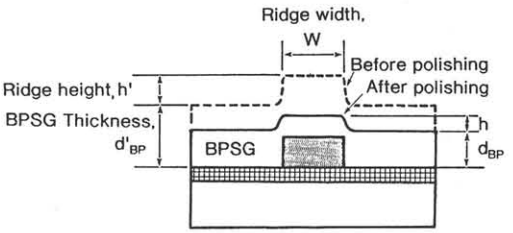

Fig. 1 A schematic illustration of a test structure used for investigating ridge width effect on a planarization rate by a mechanical polishing. The initial height of the BPSG surface ridge and the initial thickness of the BPSG around the ridges are represented as h'(=0.5μm) and d'(=0.8μm), respectively.

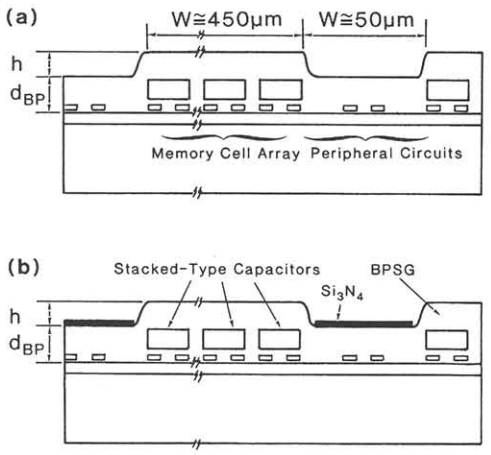

Fig. 2 Schematic illustrations of test structures used for investigating planarization processes of BPSG films on DRAM devices by (a) a mechanical polishing and (b) a NMP.

investigating a planarization process of a BPSG on DRAM devices. Here tentatively, a 1.2μm-thick BPSG was deposited on 6 inch Si-wafer having poly-Si patterns of 0.25μm-thick word (gate) lines and 0.8μm-heigth stacked-type capacitors. The BPSG film was heated and reflowed at 850°C for 30 minutes to smooth the surface. The widths of the memory cell array and the peripheral circuit areas were about 450μm and 50μm in the perpendicular direction to the word lines, respectively. The initial ridge height of the BPSG film between the memory cell array and the peripheral circuit areas was about 1.0μm.

The reflowed BPSG film on the DRAM was polished mechanically with a colloidal silica slurry for 2 to 9 minutes. For a sample used for a NMP (Fig 2(b)), the BPSG film on the peripheral circuit areas was covered with a 0.12μm-thick CVD-Si_3N_4 film by using photolithography and dry-etching processes. The test sample was polished under the same conditions as the mechanical polishing described above.

3. RESULTS AND DISCUSSION

3-1. Characteristics of Mechanical Polishing

Figure 3 shows the relation between the polishing time duration and the polished thicknesses of the reflowed BPSG and the Si_3N_4 films fabricated on flat Si-wafers. The reflowed BPSG film with the flat surface was polished at a rate of 0.15 μm/min by a mechanical polishing.

In case of the BPSG film with surface ridges (Fig. 1), the film on the ridges was polished with sacrificing the film around the ridges. The polishing rate of the film around the ridges (V_{BP}) was a constant at 0.15 μm/min, but the polishing rates on the ridges, eventually the reduction rates of the ridge height (V_h), depended on the ridge width (W). Figure 4 shows the reduction rate of the ridge height relative to the polishing rate of the BPSG around the ridges (V_h/V_{BP}) as a function of the ridge width (W). Here, the value of (V_h/V_{BP}) is called as a "planarization efficiency", meaning that a surface ridge with a large value of planarization efficiency is easily polished away without sacrificing the film around the ridge. It is found that the planarization efficiency decreases drastically with increasing the ridge width.

3-2. DRAM Surface Planarization

(a) Mechanical polishing

In the case of a 1.2μm thick reflowed BPSG film on a DRAM device, the film surface on memory cell array areas was flat, but a large step of 1.0μm in height existed between the cell array and the peripheral circuit areas (Fig. 8(a) and (b)).

Figure 5 shows the surface profiles of the BPSG film on a DRAM before and after polishing for 5 minutes by a mechanical polishing. It is found that the BPSG surface ridges are not polished away effectively due to the large width of 450μm. Figure 6 shows the ridge height (h) and the thickness of the BPSG film on the peripheral circuit areas (d_{BP}) as a function of the polishing time duration. The film on the peripheral areas was sacrificed at a rate of 0.15μm/min, thus the height of the wide ridge was only reduced at a rate of 0.04 μm/min. Hence, the planarization efficiency, (V_h/V_{BP}) was only 0.28, thereby indicating it was impossible to effectively remove the wide ridges on the DRAM by a mechanical polishing.

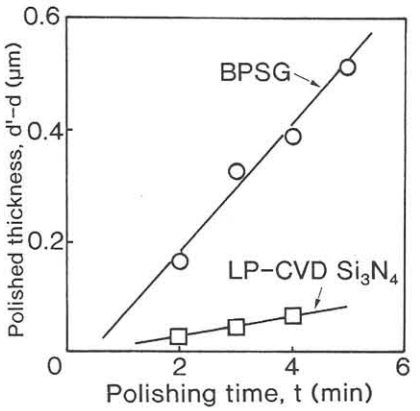

Fig. 3 Relation between the polishing time duration and the polished thicknesses of the reflowed-BPSG and the Si_3N_4 films.

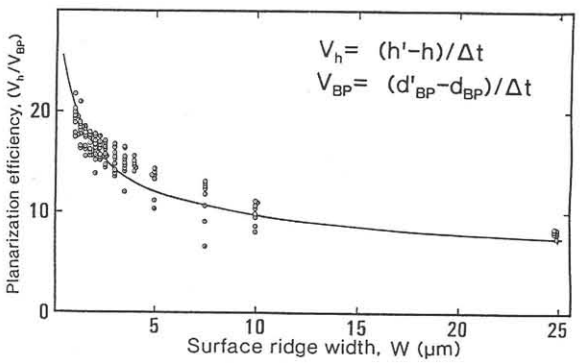

Fig. 4 Dependence of the planarization efficiency, (V_h/V_{BP}) on the surface ridge width (W) by a mechanical polishing. Δt is one minute.

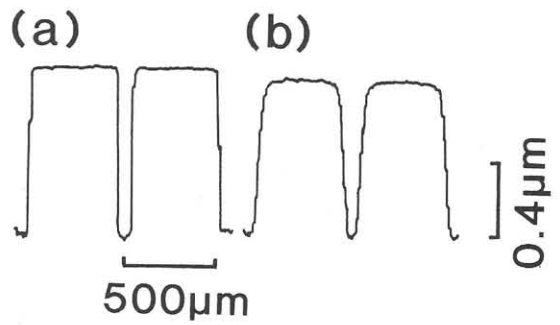

Fig. 5 Surface profiles of the BPSG film on the DRAM, (a) before and (b) after a mechanical polishing for 5 minutes.

(b) Nitride Masked Polishing

In a NMP process, a Si_3N_4 film, having a smaller polishing rate than the reflowed-BPSG film (Fig. 3), is used as a polishing protection layer. BPSG film surface except for ridge areas are covered with the Si_3N_4 film and the ridges are selectively polished away. For DRAM surface planarization, the BPSG film surface on the peripheral circuit areas are covered with the Si_3N_4 film, and the wide surface ridges on the memory cell array areas are polished selectively.

Figure 7 shows the ridge height (h) and the thickness of the BPSG film on the peripheral circuit areas (d_{BP}) as a function of the polishing time duration. Here, the ridge height and the BPSG film thickness were measured after etching the Si_3N_4 polishing protection layer by a hot phosphoric acid. Since the BPSG film on the peripheral areas was not polished due to the presence of the Si_3N_4 film, the ridge height was reduced efficiently at the rate of 0.15 μm/min. Figure 8 shows cross sectional SEM micrographs of the DRAMs before and after the NMP for 5 minutes. It was confirmed that a flat BPSG film with surface ridges of less than 0.3μm in height was obtained successfully by the NMP.

4. CONCLUSION

A Nitride Masked Polishing (NMP) technique was developed, and a BPSG film having wide surface ridges, corresponding to the stacked-type memory cell array areas in DRAM devices, was sufficiently planarized to insure a tight focus margin for photolithography below deep submicron processes.

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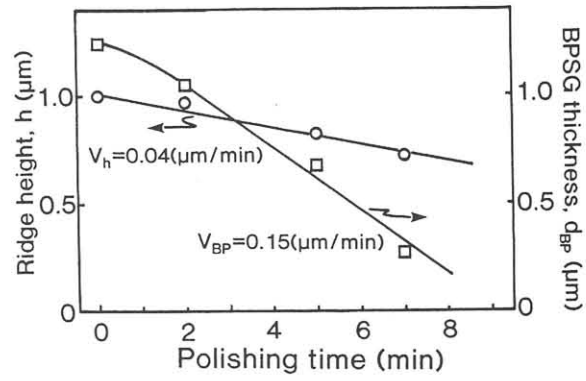

Fig. 6 Changes in the ridge height (h) and the BPSG film thickness on the peripheral circuit areas (d_{BP}) as a function of the mechanical polishing time duration.

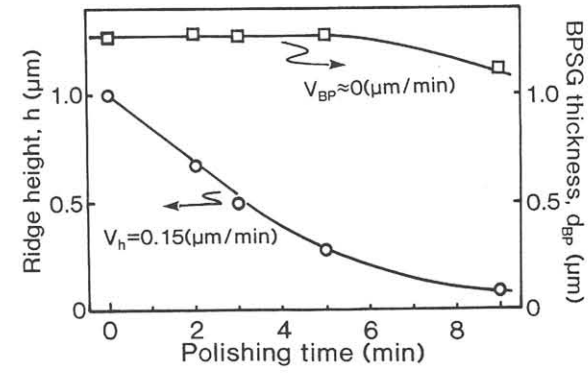

Fig. 7 Changes in the ridge height (h) and the BPSG film thickness on the peripheral circuit areas (d_{BP}) as a function of the NMP time duration.

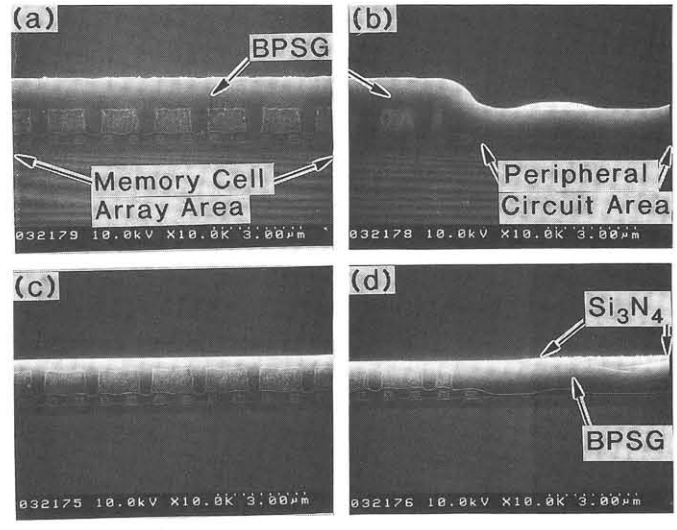

Fig. 8 Cross sectional SEM micrographs of (a) the center and (b) the edge of a stacked type memory cell array area in the DRAM structural test sample, and (c) the center and (d) the edge after the NMP for 5 min.