Extended Abstracts of the 1992 International Conference on Solid State Devices and Materials, Tsukuba, 1992, pp. 52-54

A Simple Polysilicon Thin Film Transistor Structure for Achieving High On/Off Current Ratio Independent of Gate Bias

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The ON and OFF characteristics of poly-Si TFTs described in this paper have been improved, with respect to conventional structure TFTs, by using a special device structure and a new process. To eliminate the anomalous leakage current we have used an offset gate structure while for increasing the device ON-current a fixed quantity of positive charges are introduced in the passivation layer on the top of the offset region. The presence of these charges result in accumulation of electrons at the surface which increase the surface conductivity of the offset region. Thus the proposed approach does not require any second gate electrode or use of ion implantation to achieve a high ON-current in poly-Si offset gate TFT structures.

1. INTRODUCTION

The polycrystalline silicon (poly-Si) thin film transistors (TFTs) are becoming important for active matrix liquid crystal displays (AMLCDs) and in static random access memories. In AMLCDs the poly-Si TFTs can be used for both the switching elements of the active matrix and the peripheral drive circuitry. For the former application the device leakage current must be low and must be independent of the gate bias within operating bias range. In conventional TFT the leakage current depends upon both the drain-to-source and gate-to-source bias, and its increase with gate-to-source bias has been attributed to the high electric field in the neighborhood of the drain region, which enhances the emission of electrons from traps that exist in the poly-Si film.[1] This leakage current in conventional TFTs has been characterized as the anomalous leakage current.

Although the reduction of the anomalous leakage current in the conventional (self-aligned gate) poly-Si TFT structure is difficult to achieve, this leakage current can be reduced by separating the drain and gate by an undoped offset region, Fig. 1. In this undoped region sufficient reduction of the lateral electric field takes place, which suppresses the emission of trapped carriers, and thus eliminates the anomalous leakage current. However, the undoped region introduces a high series resistance which causes a reduction of the device ON-current.

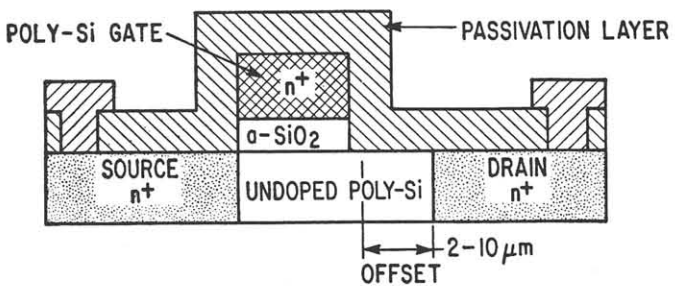

Fig. 1. TFT structure having a separation region between gate and drain contacts.

Two methods have been proposed to increase the ON-current. In one method the conductivity of the offset region is increased by doping using ion implantation.[2] In the other method a second gate electrode biased at a positive potential was used to accumulate electrons at the surface of the offset region in order to increase its conductivity.[3] These methods require either the use of ion implantation or the use of a second gate electrode. Ion implantation may be impractical or expensive for large area flat panel displays. The second gate electrode method requires additional photolithographic steps and additional electrical connections which may be difficult to implement.

In this work, we have investigated a simple method for achieving a large ON/OFF-current ratio in n-channel poly-Si TFTs, which is independent of the gate-to-source bias (V_{GS}). The below proposed

approach does not require any second gate electrode or use of ion implantation to achieve a high ON-current in poly-Si offset gate TFT structures.

2. EXPERIMENTAL

The polysilicon 100 nm thick layer was deposited either in the amorphous phase at 550°C and crystallized by thermal annealing at 600°C, or was deposited directly in the polycrystalline phase at 570°C; the substrates used were oxidized silicon wafers. The source and drain regions were doped by implanting arsenic at an energy of 40 keV and dose of $1x10^{15}cm^{-2}$. A silicon dioxide 100 nm thick film deposited by PECVD at 350°C was used as a gate dielectric layer. The 100 nm thick a-Si gate deposited by LPCVD at 550°C was also doped by arsenic implantation. The arsenic implants were activated during an 18 hrs thermal anneal at 600°C during which the a-Si gate layer was crystallized to form the heavily doped poly-Si gate. After the deposition of the passivation layer, and opening of contact windows aluminum was deposited by thermal evaporation for source/drain and gate contacts. It should be noticed that TFTs reported in this paper had a dual passivation layer on top of the offset region. First a 100 nm thick silicon dioxide was deposited by PECVD at 350°C. Then a high frequency (13.56 MHz) hydrogen plasma anneal was performed at 300°C for 60 min followed by the deposition of 177 nm thick N-rich silicon nitride film deposited by PECVD at 400°C. The layout of the completed offset gate poly-Si TFT is shown in Fig. 1. In this study, the offset region between gate and drain electrodes was between 2 and 10μm.

2. RESULTS AND DISCUSSION

An example of the output characteristic, drain-to-source current (I_{DS}) versus gate-to-source bias (V_{DS}) at different V_{GS}, is shown in Fig. 2. In a first approximation using the gradual channel equation, without accounting for the source/drain contact resistance or effective channel length, the effective field-effect mobilities (μ_{EFE}) and effective threshold voltages (V_{ET}) for different experimental conditions have been extracted in the linear region (small V_{DS}) of the output characteristics. The μ_{EFE} (slope) and V_{ET} (extrapolation at zero I_{DS}) can also be obtained from the transfer characteristics in the saturation regime, Fig. 3. In general, the μ_{EFE} and V_{ET} values deduced in the linear or saturation region for our TFTs are very similar. For poly-Si TFT having W/L=50/10 (and an offset of

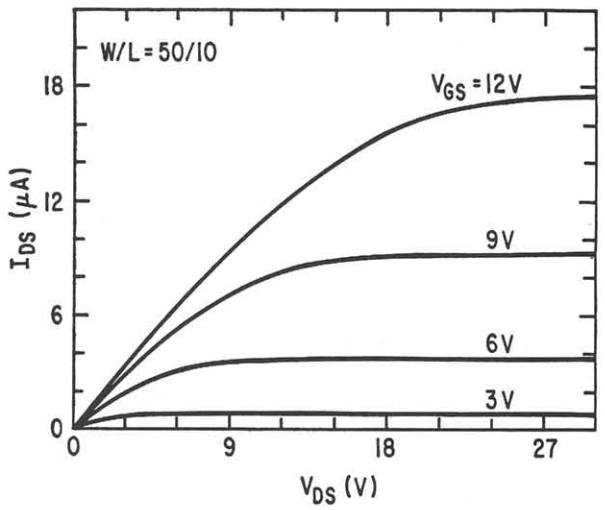

Fig. 2. Example of the output characteristic for an offset gate poly-Si TFT structure.

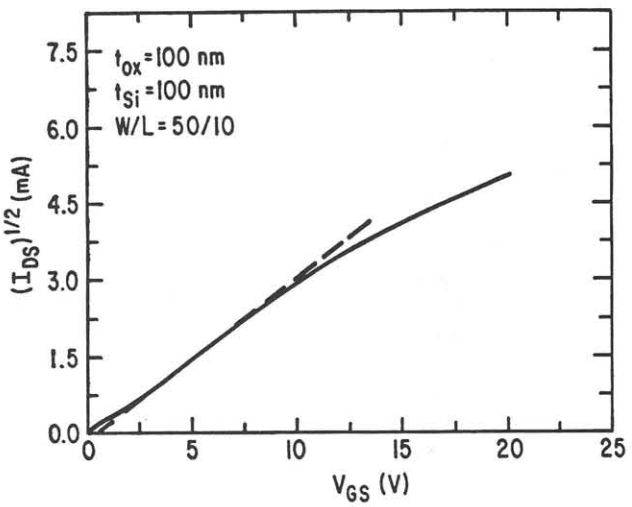

Fig. 3. Example of $(I_{DS})^{1/2}$ versus V_{GS} plot for an offset gate poly-Si TFT structure.

about 8 μm) the μ_{EFE} and V_{ET} were in the range of 3 to 10 $cm^2/Vsec$ and 0.4 to 2.0 V, respectively. An example of the transfer characteristics (I_{DS} versus V_{GS}) is shown in Fig. 4. It is clear from this figure that a low OFF-current independent of the gate bias and high ON-current can be achieved in our TFT structures. For example, OFF-current less than 2 pA per 1 μm of width, and ON-current higher than 2μA per 1 μm of width are possible with this structure.

We should also notice in Fig. 4 that an offset gate structure indeed does not exhibit an anomalous

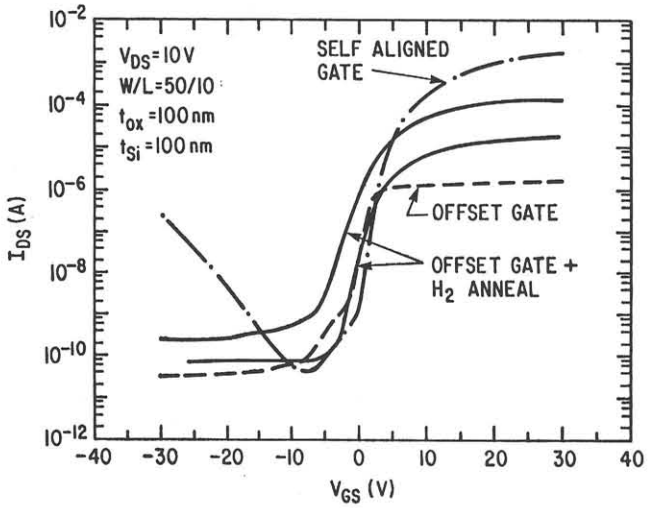

Fig. 4. Example of the transfer characteristics for different poly-Si TFT structures.

leakage current; however, due to the high series resistance of the offset region, as expected, the device ON-current is degraded in comparison to the self aligned gate TFT structure. We have found that once the offset gate TFTs are exposed to high frequency (13.56 MHz) hydrogen plasma an improvement in ON-current by two orders of magnitude was achieved. We think that during the hydrogenation positive ions are incorporated in the passivation layer. This causes electrons to accumulate in the surface of the offset region which results in a higher device ON-current. To further confirm the incorporation of positive ions in the dielectric during the high frequency hydrogenation, we have characterized n^+-i-n^+ and p^+-i-p^+ polysilicon resistors. In the former structures the resistance decreased, while in the later structure the resistance increased after the hydrogenation. A flat-band voltage of -19 V was also measured in metal/insulator/c-Si capacitors whose dielectric was exposed to a high frequency hydrogen plasma. Both these results prove for the first time that positive hydrogen ions are most likely incorporated in the dielectric during a high frequency plasma hydrogenation.

3. CONCLUSION

In conclusion, the leakage current in our TFT is approaching the liquid crystal leakage current. Further improvement of OFF-current can be achieved by improving the device structure and processing conditions. Finally, we should point out that our devices seem to be stable in time. After several weeks of storage at room temperature we did not observe any changes in the device performance.

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