## A Fabrication of Homogenious Poly-Si TFT's Using Excimer Laser Annealing

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Uniform performance in poly-Si Thin Film Transistor's (TFT's) have been successfully fabricated by excimer laser annealing. The mobility and its uniformity for n-ch TFT were  $62 \text{cm}^2/\text{V}$ 's and less than  $\pm 5\%$  at  $3\sigma/\text{ave}$ . To achieve excellent uniformity with high performance, we combined step annealing that uses two energy levels, and small pitch annealing that moves a beam forward by a small pitch. The method can improve the surface morphology and uniformity of grain size in poly-Si.

#### 1. Introduction

The poly-Si TFT is expected to provide driving circuits for large-area devices such as image sensors and LC displays. Though an excimer laser crystallized poly-Si TFT has high performance<sup>1)</sup>, there have been few reports about its uniformity. An energy deviation within a beam causes variation of grain size in the poly-Si and the crystallinity degrades in the overlapped area between beams<sup>2)</sup>. These would degrade uniformity of TFT performance. Moreover, after this crystallization, surface morphology is poor and the roughness increases as the laser energy is increased. We have evaluated the dependence of uniformity on laser energy and beam scanning pitch. As a result , both step annealing<sup>3)</sup> that uses two energy levels, and small pitch annealing<sup>4)</sup> that moves a beam forward by a small pitch, have been effective for uniformity.

In this paper, to obtain excellent uniformity for CMOS circuits, we have combined step annealing and small pitch method, and optimized step annealing conditions with small pitch annealing.

### 2. Experiments

An 100nm-thick a-Si film was deposited by LPCVD on a quartz substrate and then crystallized by excimer laser(KrF). The size of the beam was about  $7 \times 7$ mm<sup>2</sup> and the energy variation was less

than  $\pm 5\%$  within the beam. Step annealing consisted of an initial low energy shot E<sub>1</sub> followed by a 2nd higher energy shot E<sub>2</sub>. In the single annealing process,only E<sub>2</sub> was used. The scanning pitches were 0.5mm and 6.5mm. Using the crystallized film, co-planar type n-ch and p-ch TFT's were fabricated below 600°C. The TFT size was W/L =  $50\mu$ m/10 $\mu$ m. Mobility ( $\mu$ ), minimum leakage current (I<sub>MIN</sub>), threshold voltage (V<sub>TH</sub>) were evaluated. Grain size was estimated using SEM views taken after Secco etching and X-ray diffraction measurement was taken to evaluate crystallinity. The surface roughness of a film was evaluated by AFM (Atomic Force Microscopy).

# 3. Effects of step annealing

Fig.1 shows the dependence of the performance and uniformity on the laser energy E with 6.5mm pitch. Though high performance was achieved at  $E = 450 \text{mJ} \cdot \text{cm}^{-2}$ , uniformity of mobility  $\mu$  was poor. On the other hand, step annealing ("step anneal") achieved good uniformity in  $\mu$  over a substrate. This indicates that step annealing method can improve uniformity of grain sizes.From SEM observation, step annealing improved the reduction of grain sizes in the overlapped area between beams, and uniformity within a beam. Fig.2 shows the AFM images for single and step annealing. With step annealing, surface roughness was reduced by 40% compared with the single annealed case.



Fig.1. The dependence of performance on the laser energy E(6.5mm-pitch). Step annealing used a 1st low  $E_1$  (270mJ·cm<sup>-2</sup>) followed by a 2nd higher  $E_2$  (450mJ·cm<sup>-2</sup>).







### 4. Optimization on step annealing conditions

Next, we optimized step annealing conditions with small pitch (0.5mm). Fig.3 shows the dependence of X-ray intensity on  $E_1$ . The intensity corresponds to grain size. For  $E_2 = 450 \text{mJ} \cdot \text{cm}^{-2}$ , the intensity abruptly reduced at  $E_1 = 240 \text{mJ} \cdot \text{cm}^{-2}$ and gradually increased above  $E_1 = 270 \text{mJ} \cdot \text{cm}^{-2}$ . At point A, grain size was reduced due to a limitation by many little nuclei prepared by  $E_1$ . However from SEM and AFM observations, the surface roughness and the deviation of grain size were found to be minimized at this point. On the



Fig.4. The dependence of mobility on the 1st energy  $E_1$  with small pitch ( $E_2 = 450$  mJ·cm<sup>-2</sup>).

other hand , when  $E_2$  was as high as 650mJ·cm<sup>-2</sup>, the reduction of grain size was not observed at any  $E_1$ . Near point A, we could expect the uniform performance of TFT's.

Fig.4 shows the dependence of  $\mu$  on E<sub>1</sub> at E<sub>2</sub> = 450 mJ·cm<sup>-2</sup>. The mobility reduced as E<sub>1</sub> increases, but above E<sub>1</sub> = 270 mJ·cm<sup>-2</sup> its value and uniformity were improved. E<sub>1</sub>'s below 270 mJ·cm<sup>-2</sup> have no effect on uniformity.

Fig.5 shows the dependence of  $\mu$  on E<sub>2</sub> (E<sub>1</sub> = 270mJ·cm<sup>-2</sup>). Uniformity was improved as E<sub>2</sub> increased, but degraded above E<sub>2</sub> = 520mJ·cm<sup>-2</sup>.

Excellent uniformity was derived at  $E_1/E_2 = 270/450 \text{ mJ} \cdot \text{cm}^{-2}(\Delta \mu = \pm 5\%, \Delta \text{V}_{\text{TH}} = \pm 22\%, \Delta \text{I}_{\text{MIN}} = \pm 22\%$  at  $3\sigma/\text{ave.,n-ch}$ ). Fig.6 shows I<sub>D</sub>-V<sub>G</sub> characteristics in the above condition. TFT performance was excellent for both n-ch ( $\mu = 62 \text{ cm}^2/\text{V} \cdot \text{s}, \text{V}_{\text{TH}} = 0.8\text{V}, \text{I}_{\text{MIN}} = 5\text{pA}$ ) and p-ch ( $\mu = 45 \text{ cm}^2/\text{V} \cdot \text{s}, \text{V}_{\text{TH}} = -2.7\text{V}, \text{I}_{\text{MIN}} = -2\text{pA}$ )types. CMOS shift resistors composed of these TFT's showed an







excellent performance (the speed was over 1MHz at 8V supply voltage)<sup>5)</sup>.

### 5. Discussion - Annealing mechanisms

Figure7 speculates the mechanism of step annealing. In single annealing, using low E's (a) the film has good surface morphology but many defects left, while using high E's (b) the film has poor morphology but less defects. In step annealing the 1st shot with E<sub>1</sub> prepares a smooth surface, leaving many defects in the film. Secondly, a high E<sub>2</sub> does not melt the crystalline nuclei but melts amorphous-like defective parts (c). As a result, the film has smoother morphology than the single annealed one(b), and have grains of uniform size because of the presence of many little nuclei prepared by E<sub>1</sub>. Even if there are energy deviations within a beam, these prepared





nuclei could control grain sizes to be small and uniform over poly-Si film.

The effects of step annealing ocurred only at an appropriate combination of  $E_1$  and  $E_2$ . This is explained as follows. The excessively low  $E_1$  can not prepare nuclei that do not melt easily under 2nd shot  $E_2$ . And using high  $E_1$ , the roughness in the film degrades. On the other hand, the excessively high  $E_2$  would cancel a film structure prepared by  $E_1$ . Therefore, we must control the crystallinity of nuclei by an appropriate combination of  $E_1$  and  $E_2$  for uniformity.

## 6. Summary

With a single shot, the TFT performance was best at  $450 \text{mJ} \cdot \text{cm}^{-2}$ , but the extremely large variations rendered this device impractical for most applications. To improve uniformity we proposed a combination of small pitch annealing and step annealing. With  $E_1/E_2$  of 270/450 mJ·cm<sup>-2</sup> the surface roughness and the deviation of the grain size were minimized. As a result excellent uniformity in TFT performance was achieved.

### References

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